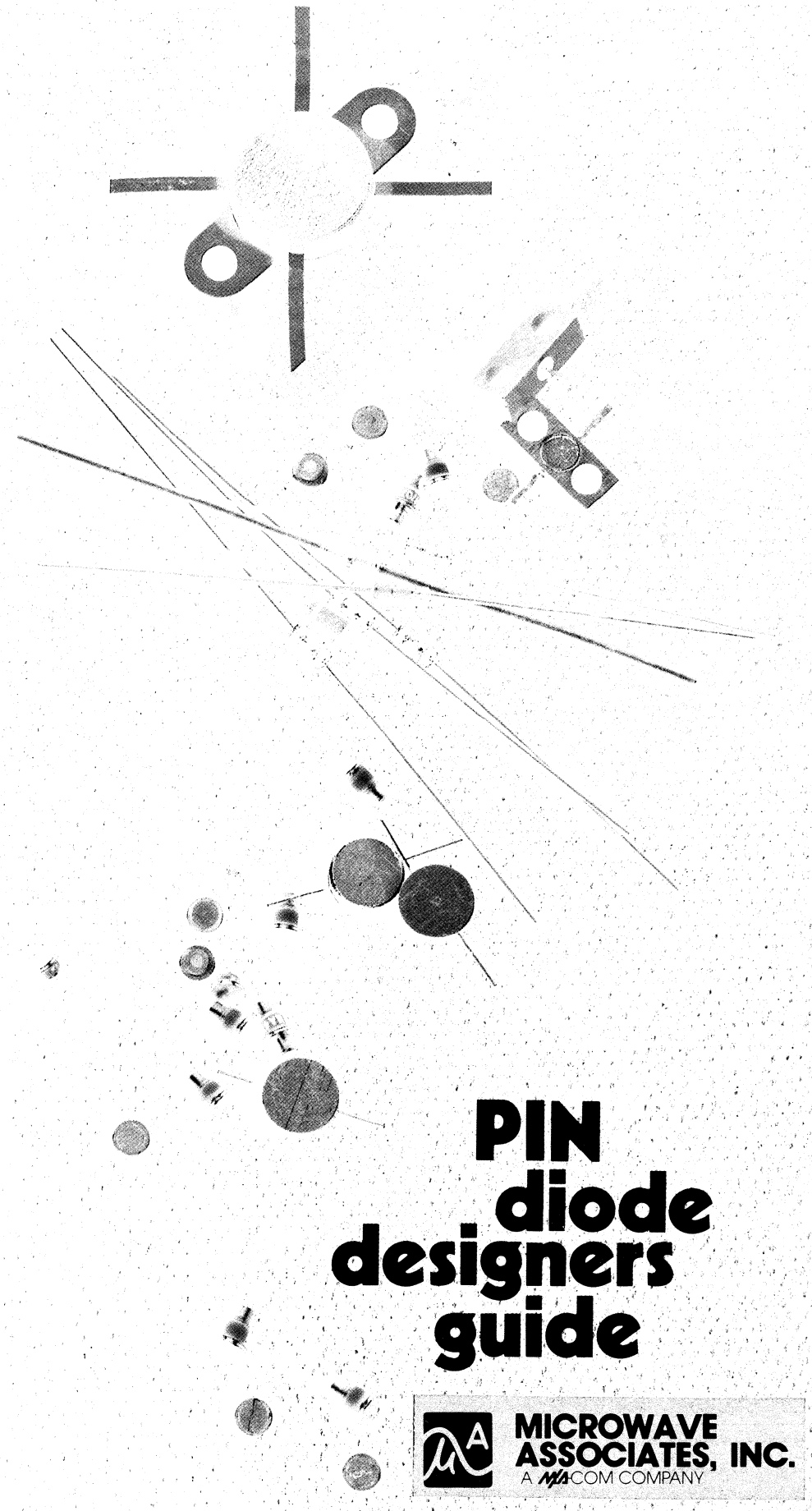


PIN diode designers guide

MICROWAVE ASSOCIATES, INC.
A MACOM COMPANY

introduction

Microwave Associates is the world's leading manufacturer and custom designer of microwave semiconductor devices. For more than 25 years, we have been developing and manufacturing state-of-the-art silicon and gallium arsenide devices for a wide variety of uses in both commercial and military applications. The established product lines include power generation and amplification diodes and transistors, receiving diodes of all types (mixers and detectors), special products such as silicon material, diode packages and MIS capacitors, and a wide variety of signal control devices. PIN diodes are in the control devices category.

The modern, well-equipped facilities and advanced processing techniques of the Silicon Products Group, an operating group of Microwave Associates, have provided a basis for the development of a high level PIN diode technology. Standard and custom designed beam-lead, chip and packaged PIN diodes are available for the entire RF and microwave spectrum. In the final chapter of the PIN Designers' Guide a complete standard PIN diode matrix is presented for use in the design of low, medium and high power RF switches, limiters, duplexers, phase shifters and attenuators. A wide variety of parameter options and case enclosures is available.

The PIN Designers' Guide is meant to be a useful reference and selection aid for the RF circuit designer. Included are not only practical handling techniques for chip devices and detailed descriptions of pertinent diode measurements, but also an in-depth chapter on the device physics of PIN diodes (Chapter 1). The actual design procedures, performance trade-offs and functional details are discussed for the design of 17 different switch types, limiters and attenuators (Chapter 10). Driver considerations, package parasitics and PIN diode quality and reliability are each treated in separate sections.

The purpose of the PIN Designers' Guide is to serve the needs of the customer by providing an industrial reference on PIN diodes. Instead of merely being a collection of data sheets and application notes, this complete overview treats device theory, device handling, applications, design procedures and device selection.

Microwave Associates has achieved technological leadership and expertise in PIN devices through the efforts of a highly skilled team of technical and marketing specialists who are a part of a multi-national team created to serve you, the customer. Our charter is to provide a reliable quality product at a reasonable price. To achieve this, our technical staff is continually at work developing new device concepts and our sales and applications personnel are standing by to serve the demands of a fast growing industry.

contents

contents

contents

contents

contents

contents

device physics of PIN diodes

device physics of PIN diodes

1

1.1 DISCUSSION

The purpose of this chapter is to provide enough basic device concepts to facilitate use of the following chapters on PIN diode applications. For individuals interested in more detail on the device properties of PIN diodes, excellent texts by White[1] and Watson[2] are available.

1.2 SILICON JUNCTION DIODES

The fundamentals for all silicon junction microwave diodes are found in the physics of a PN junction. Semiconductors can be doped either N or P by adding impurities to the basic crystal lattice. Impurities such as arsenic, phosphorus and antimony in silicon are of the N type and introduce a loosely-bound electron into the crystal lattice. Impurities such as boron, gallium and aluminum in silicon are of the P type and introduce a loosely-bound hole, or missing electron, into the crystal lattice. N material has negatively charged electrons as the majority carrier of electrical current, while P material has positively charged holes as the majority carrier. Due to thermal excitation of hole electron pairs, some holes are present as minority carriers in N material and some electrons are present as minority carriers in P material. Silicon material which is without impurities is known as intrinsic silicon. In intrinsic silicon, holes and electrons are present in equal numbers, which are governed by thermal generation.

In general, microwave devices have doping levels which are uniform in the y-z plane and are therefore a function of x only. For N material, the doping density is a donor density, N_D (x), and for P material, it is an acceptor density, N_A (x). A PN junction occurs when the quantity N (x) = N_D (x) — N_A (x) changes sign or when the material changes from N-type to P-type.

The current-voltage characteristic of a PN junction is shown in Figure 1.2-1. When the P side is biased positive with respect to the N side, the device will conduct current easily. This region is often characterized by specifying a maximum forward voltage (V_f) drop for a specific forward current (I_f). When biased in the opposite way, the device blocks DC current for reverse voltages less than the junction breakdown voltage. In this region, the device is often characterized by a maximum leakage current at a specific reverse voltage (V_r). At the breakdown voltage, carrier multiplication by impact ionization occurs, so that large increases in current are obtained for small increases in terminal voltage. It is customary to specify the breakdown voltage (V_b) as the voltage at which the reverse current (I_r) is 10μA.

The doping profile N (x) for an idealized, uniformly doped abrupt junction diode is shown in Figure 1.2-2(a). When N and P materials are placed in intimate contact with each other, there are more free electrons on the N side than on the P side. Electrons start flowing by diffusion from the N side to the P side. In similar fashion, the holes start to flow from the P side to the N side. In normal N or P material, the charge of mobile carriers exactly balances the charge of the donor or acceptor atoms fixed in the lattice. When the mobile electrons leave the N material near the junction, they leave behind positively charged donor atoms fixed in the silicon lattice. In similar fashion, the holes in the P material flowing to the N material leave behind negatively charged acceptor atoms in the lattice. The effect of this is to build up a dipole space-charge layer which retards further diffusion of electrons from the N side to the P side as shown in Figure 1.2-2(b). The dipole layer adjusts itself so that there are equal quantities of electrons and holes crossing the junction in each direction. Minority carrier electrons which diffuse to the edge of the space-charge layer will fall down the potential barrier into the N material. Similarly, there are energetic electrons on the N side which can overcome the potential barrier and cross over to the P side. At equilibrium, these two carrier streams are exactly equal. The net current is zero and the net terminal voltage is also zero.

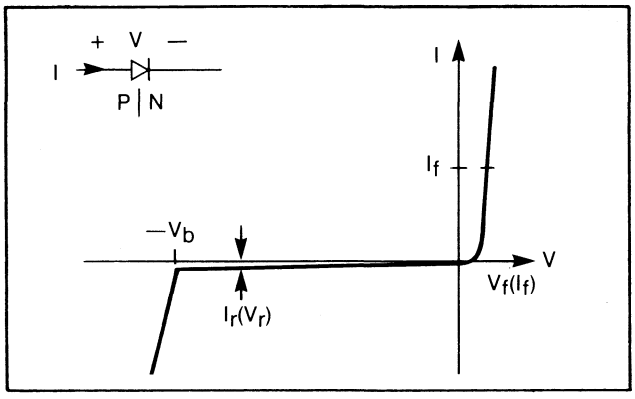


FIGURE 1.2-1 CURRENT VS VOLTAGE CHARACTERISTIC OF A TYPICAL PN JUNCTION DIODE

(1) White, J.F., "Semiconductor Control", Artech House, 1977.
(2) Watson, H.A., "Microwave Semiconductor Devices and Their Circuit Applications", McGraw Hill, 1969.

device physics of PIN diodes

2

The energy band diagram for the PN junction at zero bias is shown in Figure 1.2-3. In the figure, E_C is the conduction band energy, E_V is the valence band energy and E_F is the Fermi energy, or chemical potential. For silicon, the potential barrier Φ_O at zero bias is approximately 0.7 volt. Forward bias reduces this barrier and allows more majority carriers to cross the space charge or depletion region. Once across, they are then minority carriers on that side of the junction. This phenomenon is called minority carrier injection. Reverse bias increases the barrier and reduces the flow of majority carriers across the junction. Reverse leakage occurs when minority carriers drift to the depletion region edges and are pulled across it by the electric field. An additional component of reverse leakage current arises from carrier generation within the space-charge region.

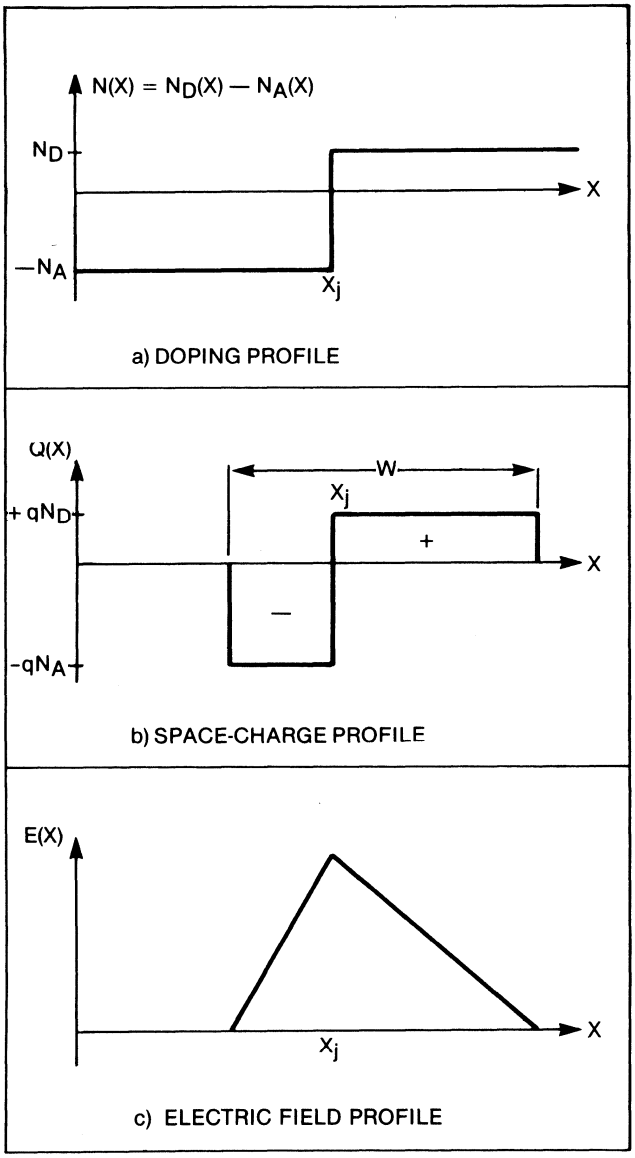


FIGURE 1.2-2 DOPING PROFILE, SPACE-CHARGE PROFILE AND ELECTRIC FIELD PROFILE FOR AN ABRUPT UNIFORM DOPING PN JUNCTION

Using Poisson's equation, one can integrate the charge distribution of Figure 1.2-2(b) to determine the electric field across the depletion region. The electric field E (x) is shown in Figure 1.2-2(c). Note that the peak electric field occurs at the PN junction. When this peak field reaches the threshold value for impact ionization, the PN junction goes into avalanche breakdown. Thus, knowing both the threshold field for silicon (which is a function of doping level) and the electric field distribution, one can calculate the breakdown voltage of a given PN junction. An additional integration of the electric field yields the voltage drop, or potential, across the junction. The voltage provides the boundary condition which fixes the specific dimensions of the space-charge, or depletion, region. As the voltage increases, the space-charge region widens to support the voltage. In this manner, the width of the space-charge region is a function of voltage.

Under reverse bias, for a given applied voltage (V) there is an equilibrium value (W) for the width of the space-charge region. The space-charge region approaches equilibrium at a rate given by the dielectric relaxation time (τ_d) of the silicon. The dielectric relaxation time is the time in which a charge unbalance decays to 1/e of its initial value and is given by:

$$\tau d = \frac{\epsilon}{\sigma} \qquad (1\text{-}1)$$

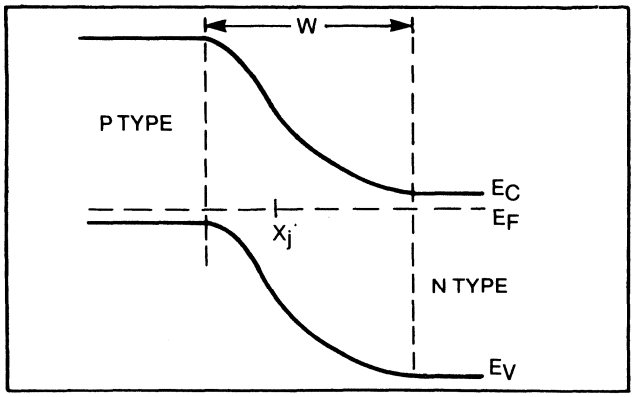


FIGURE 1.2-3 ENERGY BAND DIAGRAM FOR ABRUPT UNIFORM DOPING PN JUNCTION AT ZERO BIAS

where σ is the conductivity of the silicon junction region and ϵ is the electric permittivity of silicon. At low frequencies, when the RF period is substantially greater than τ_d, the depletion region width is defined by the instantaneous applied voltage. At high frequencies, when the RF period is substantially less than τ_d, the equilibrium depletion width cannot follow the instantaneous RF voltage. Figure 1.2-4 shows the variation of τ_d with silicon resistivity. A typical tuning diode has an active region resistivity of 0.5 ohm-cm, while a PIN diode has an active region resistivity of several hundred ohm-cm or more. This resistivity difference leads to very different RF properties of the two device types.

Minority carriers injected into both the P and N layers at forward bias cannot be extracted with time constants as fast as the dielectric relaxation time of the material. These carriers must either be withdrawn by reverse current through the diode or be allowed to decay naturally with their own time constant.

The reverse bias PN junction diode has been shown to have a depletion region whose width (W) is a function of doping level and applied voltage. On an AC small-signal basis, the diode appears electrically as a plane parallel plate capacitor with plate separation W. The junction has a capacitance given by:

$$C_j = \frac{\epsilon A}{W} \qquad (1\text{-}2)$$

where C_j is the junction capacitance and A is the device area. Using Equation 1-2 and the expression

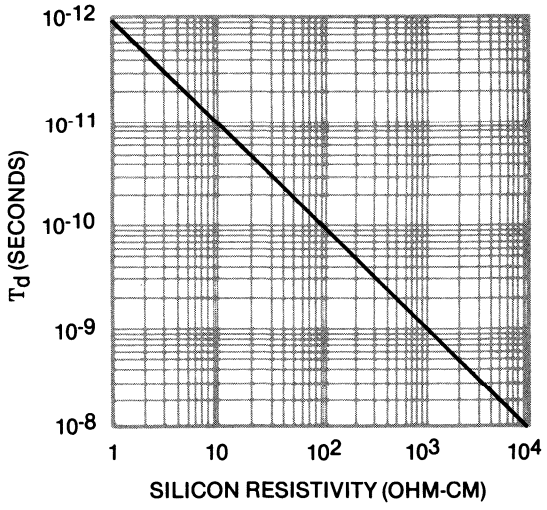


FIGURE 1.2-4 DIELECTRIC RELAXATION TIME τ_d VS. RESISTIVITY FOR SILICON

for W as a function of voltage, the capacitance for a uniformly doped abrupt PN junction is given by:

$$C_j(V) = \frac{A}{2}\left[\frac{2g\epsilon}{(\Phi_o - V)(1/N_A - 1/N_D)}\right]^{1/2} \qquad (1\text{-}3)$$

where q is the electronic charge, Φ_o is the contact potential, and V is the applied voltage with the polarity shown in Figure 1.2-1.

For a P+N junction (i.e., the P side very heavily doped) Equation 1-3 simplifies to:

$$C_j(V) = \frac{A}{2}\left[\frac{2q\epsilon N_D}{(\Phi_o - V)}\right]^{1/2} \qquad (1\text{-}4)$$

For a linearly graded junction, where the impurity distribution at the junction is given by:

$$N(x) = (a)(x) \qquad (1\text{-}5)$$

where a is a constant.

The junction capacitance is given by:

$$C_o(V) = \epsilon A\left[\frac{qa}{12\epsilon(\Phi_o - V)}\right]^{1/3} \qquad (1\text{-}6)$$

Thus, for an abrupt uniform junction, $C_j(V) \propto V^{-1/2}$. For a linearly-graded junction, $C_j(V) \propto V^{-1/3}$. The simplified expressions are, for reverse voltages, many times greater than Φ_o, which, for silicon, is approximately 0.7 volts. By varying the junction doping profile, the functional dependence of junction capacitance on voltage can be tailored.

Although the depletion region acts as a low-loss capacitor, the undepleted semiconductor regions act as resistors. Practical device structures are designed to have the undepleted semiconductor regions as heavily doped as possible in order to minimize losses. The doping profile of a microwave P+N junction diode is shown in Figure 1.2-5. This profile would be appropriate for a tuning or multiplier diode. Ideally, there would be an appropriate resistivity N layer sandwiched between two heavily doped N+ and P+ layers, with very abrupt transitions between regions. However, in practice, one starts with an N on N+ silicon epitaxial slice. Typically, this slice would have a 4- to 10-micron thick layer of 0.5 to 5 ohm-cm resistivity silicon epitaxially grown on a 10 mil thick, arsenic-doped silicon substrate slice with resistivity of .001 ohm-cm. The P+ layer is formed by diffusing elemental boron into the front

surface of the slice at 1050° to 1200°C for a precise time. The diffusion process results in an impurity distribution which is approximately error function in nature. During the P+ diffusion process and any subsequent high temperature processing, the NN+ junction becomes more graded, due to diffusion from the heavily doped substrate to the N layer.

1.3 PIN DIODES

A PIN diode is a form of P+NN+ device with an intrinsic active region such that $N_D(x) = N_A(x) = 0$ in the N layer. In practice, it is impossible to obtain and maintain through processing truly intrinsic material. Thus, most PIN diodes have layers which are slightly N-type or P-type. Consider a device with a very lightly doped N region. Figure 1.3-1(a) shows the doping profile for such an ideal PIN diode. Note that there are really two junctions: a P+N⁻ junction and an N⁻N+ junction. At zero bias, a depletion region will form at the P+N⁻ junction to accommodate the contact potential Φ_O. If the doping in the N⁻ layer is sufficiently small, and the width is small, the zero-bias depletion region may extend all the way to the N+ region. Such a device is said to have a zero-bias punchthrough. A more typical situation is that the zero-bias depletion region extends only slightly into the N⁻ region. As reverse bias increases, the depletion region grows wider and wider until it reaches through to the N+ region. At this point, the depletion region will not increase further in width, since for very little increase in W, large amounts of space charge can be obtained for the space-charge region. The voltage at which this occurs is called the punchthrough voltage (V_P). Figure 1.3-1(c) shows the electric field profile across the PIN diode junction. The lower the doping level in the I region, the more constant the electric field is across the I region. The slope of the electric field is given by $q N_D/\epsilon$.

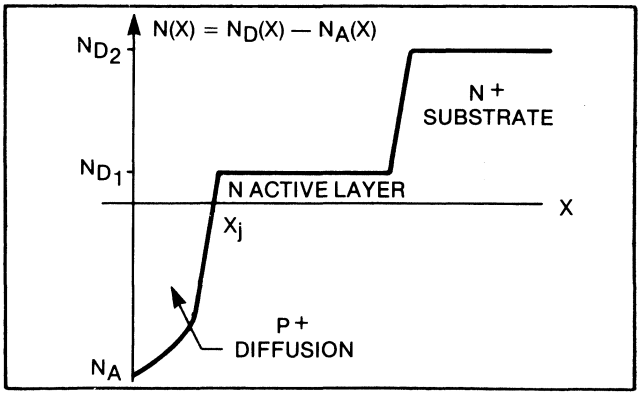


FIGURE 1.2-5 DOPING PROFILE N (x) FOR A MICROWAVE P+N N+ DIODE

Figure 1.3-2 shows the low frequency capacitance vs voltage characteristic for a typical PIN diode on a log-log plot. For voltages less than the punchthrough voltage, the device behaves similarly to a uniformly doped P+N junction. At the punchthrough voltage, the capacitance vs voltage variation changes to a very shallow slope. An ideal PIN diode would have zero slope or a constant capacitance with voltage for all voltages greater than V_P. In practice, the slope of the region is no greater than 0.15.

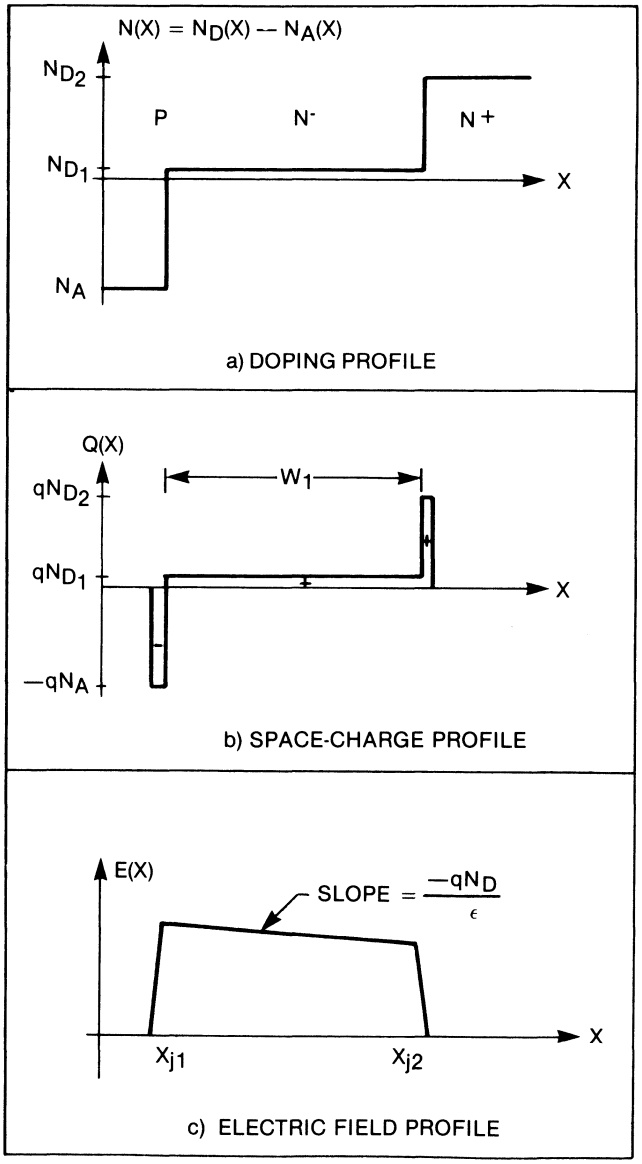


FIGURE 1.3-1 DOPING PROFILE, SPACE-CHARGE PROFILE, AND ELECTRIC FIELD PROFILE FOR AN IDEAL PIN DIODE WITH AN N— I-REGION

Since the electric field is almost uniform across the active region, and the voltage is the integral of the electric field across the junction, one can estimate the breakdown voltage of PIN diodes from a knowledge of the threshold field for avalanche breakdown. For lightly doped silicon the threshold field is approximately 2 (10^5) volts/cm. Thus, an approximation for the breakdown voltage of a PIN diode becomes:

$$V_B = E_{max} W_1 = 2(10^5)(W_1) \quad (1\text{-}7)$$

when W_1 is the I-region width in centimeters. For the I-region width specified in microns, V_b is approximately 20 volts per micron. Typical PIN diodes have I-region widths ranging from 1.5 to 150 microns or V_b ranging from 30 to 1500 volts.

1.4 PIN DIODE STRUCTURES

At Microwave Associates, PIN diode chips are made in four distinct structures: passivated mesa, CERMACHIP™, planar and beam lead.

The passivated mesa structure shown in Figure 1.4-1 is the most common construction for PIN diodes in the 30 to 300 volt breakdown range. The mesa structure allows the active I-region to resemble very closely a parallel-plate capacitor with minimum fringing capacitance to the substrate. The mesa structure also maximizes the surface breakdown voltage. This results in device breakdown voltages very close to the bulk breakdown voltage. A thermal oxide is used as the surface passivation layer for maximum reliability. The ohmic contact metallization of titanium tungsten and gold is a dry refractory metal contact system well known for high reliability. In order to retain full reliability, this type of chip should be used in hermetically sealed packages or circuit modules.

The CERMACHIP™ construction shown in Figure 1.4-2 is a process unique to Microwave Associates. The basic geometry of the chip is the same as for the passivated mesa. The major difference is in the passivation: a thick hard-glass passivation is used in place of the thermal oxide of the passivated mesa type. The hard glass passivation allows the CERMACHIP™ to replace a fully packaged hermetically sealed diode chip in many applications. This reliability has been proven by extensive RF and DC testing which included humidity testing. Because of process limitations, only chips with large I-region thickness (2 mils or greater) and active-region diameters greater than 6 mils can be made with the CERMACHIP™ process. For this reason, CERMACHIP™ is used predominantly for high-power applications such as high-power switches and phase shifters. The CERMACHIP™ devices can be used directly, without any regard to mounting in a hermetically sealed enclosure.

A planar PIN diode chip is shown in Figure 1.4-3. This type of device is made by diffusing boron through a window in the thermal oxidation passivation to form the junction. This is the most common form of fabrication for low-frequency diodes and transistors. The boron diffuses into the silicon under the edge of the oxide mask and in the open window. For microwave purposes, planar devices have two major short-comings. First, the PN junction depletion region is shaped like a plane-parallel plate capacitor in the center, but is cylindrically shaped at the

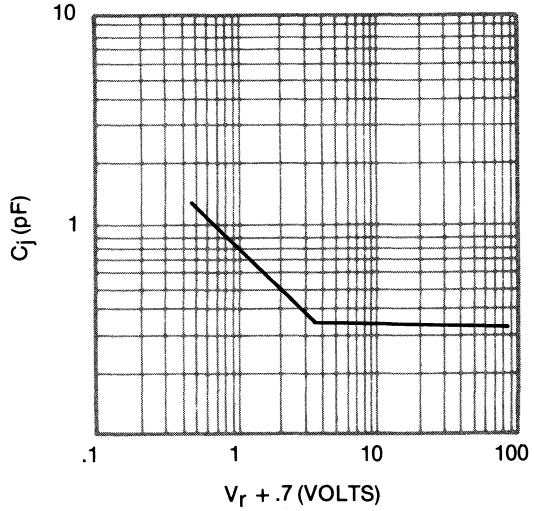


FIGURE 1.3-2 TYPICAL JUNCTION CAPACITANCE, C_j, VS. REVERSE VOLTAGE, V_r, FOR A PIN DIODE WITH A 2 MIL THICK I-REGION

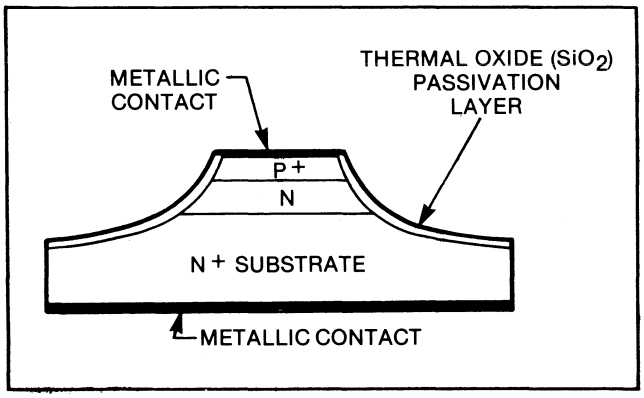


FIGURE 1.4-1 THERMAL OXIDE PASSIVATED MESA CONSTRUCTION PIN DIODE

edges. The cylindrical junction at the edges reduces the voltage breakdown considerably from a mesa device with an I-region of the same thickness. Second, the inactive silicon surrounding the junction produces extra fringing capacitance. It also stores charge, thereby reducing switching speed in comparison to an equivalent-sized mesa device. However, the planar device has unique properties in the forward-bias direction which make it ideal for attenuator applications. The series resistance vs current characteristic is linear on a log-log plot over a wide dynamic range of forward-bias currents. This situation, coupled with the fact that planar devices are inexpensive to fabricate, makes planar PIN diodes extremely useful for low frequency or attenuator applications.

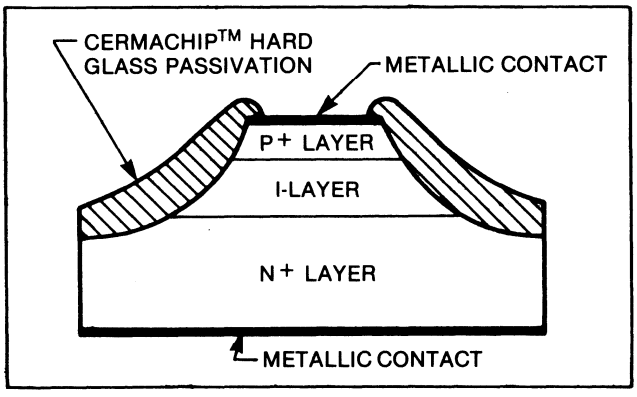


FIGURE 1.4-2 CERMACHIP™ CONSTRUCTION PIN DIODE

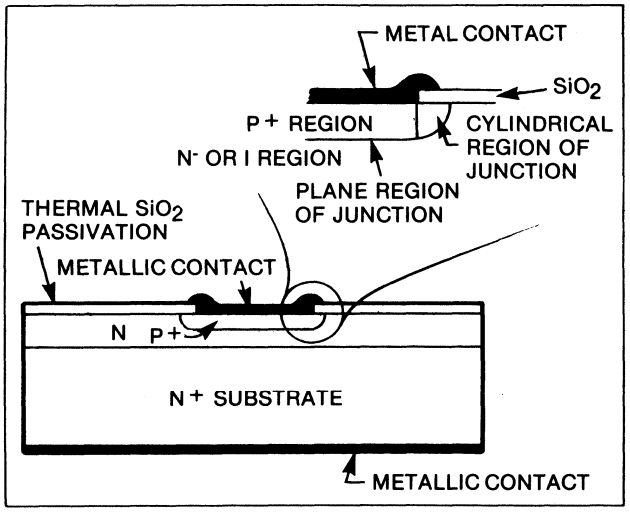


FIGURE 1.4-3 PLANAR CONSTRUCTION PIN DIODE

Figure 1.4-4 shows the construction of a beam-lead PIN diode. A beam-lead diode is a planar PIN diode with both contacts on the same side of the silicon wafer. During the metallization process, a large-area, thick gold beam is attached to each active contact. The silicon between devices is then etched away, leaving a planar chip with two co-planar beam-like contacts to the device. The device is particularly suited for series mounting in hybrid IC circuits. The principal advantages of beam-lead devices are that they can be made extremely small with very low junction capacitance, and that the mounting configuration results in a minimum of lead inductance.

PIN diodes are available as chip devices or mounted in a variety of microwave packages. A typical cross-section of a passivated mesa PIN chip in a ceramic package is shown in Figure 1.4-5. The semiconductor diode chip is soldered to the package with AuSi eutectic solder or AuGe solder. A gold-to-gold thermocompression wedge bond is used to attach the gold lead from the package flange to the top chip contact and back to the package flange. The packages provide a hermetically sealed environment for the chip which permits easy mounting in coaxial and waveguide circuits. The electrical effect of the package is to add a shunt package capacitance (C_P) across the junction and a lead inductance (L_S) in series with the junction. Both of these effects limit bandwidth and must be accounted for in circuit designs. C_P and L_S vary from package to package and are typically a few tenths of a picofarad and a few tenths of a nanohenry, respectively. Chapter 6 will provide a detailed discussion on package parasitics.

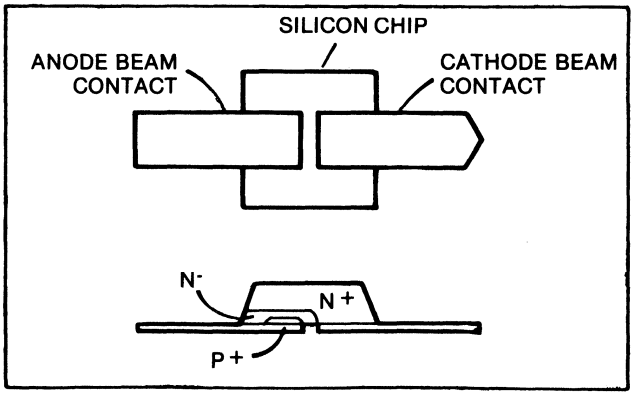


FIGURE 1.4-4 BEAM-LEAD CONSTRUCTION PIN DIODE

1.5 EQUIVALENT CIRCUITS

Figure 1.5-1 shows the equivalent circuit for a packaged PIN diode in the forward and reverse biased states.

Figure 1.5-1(a) shows the equivalent circuit for a reverse-biased PIN diode as a capacitor in series with a resistor. The capacitance (C_j) is given simply by:

$$C_j = \frac{\epsilon A}{W_1} \qquad (1\text{-}8)$$

where W_1 is the width of the I-layer. This expresses what is to be expected for all reverse voltages greater than the device's punchthrough voltage. However, for PIN diodes, most RF frequencies are of shorter period than the dielectric relaxation time and Equation 1-8 is valid for all reverse voltages down to zero volts. The diode series resistance (R_S) is the sum of all the resistances of the undepleted silicon regions and the contact resistance of both ohmic contacts. For well designed PIN diodes, R_S ranges from 0.2 to 3.0 ohms, depending on junction size. Thus, the PIN diode can be represented as a fixed-value, low-loss capacitor in the reverse-bias state. For appropriate values of capacitance, the reverse-biased PIN diode blocks RF transmission when placed in series with a transmission line, and permits RF transmission when placed in shunt with a transmission line.

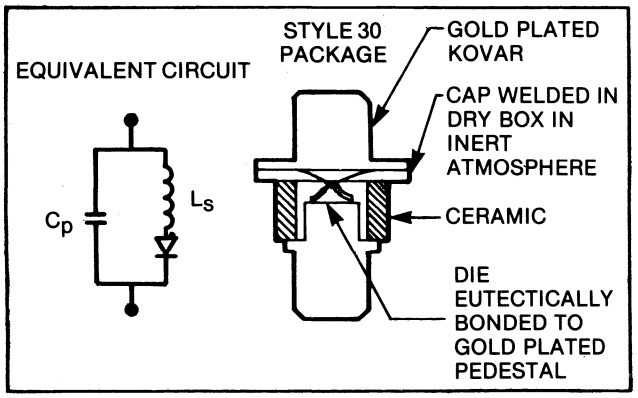


FIGURE 1.4-5 INTERNAL CONSTRUCTION OF A PACKAGED DIODE SHOWING EQUIVALENT CIRCUIT

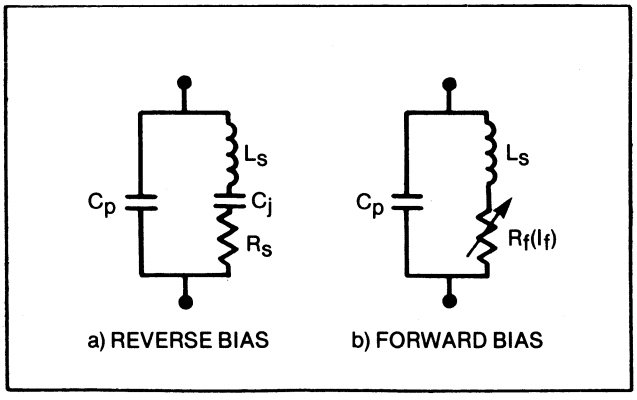


FIGURE 1.5-1 EQUIVALENT CIRCUIT OF FORWARD AND REVERSE BIASED PACKAGED PIN DIODE

Figure 1.5-1(b) shows the equivalent circuit of a forward biased PIN diode as a resistor (R_f) which is a function of the DC forward current (I_f). In forward bias, both holes and electrons are injected into the I-layer. The mobile carriers form a conductive plasma whose resistivity depends on the carrier density obtained from the injection process. Because the forward current injects carriers into the I-region to modulate its conductivity, the effect is known as conductivity modulation.

The forward resistance (R_f) may be expressed as:

$$R_f = R_I + R_{Sf} \qquad (1\text{-}9)$$

where R_I is the resistance due to the I-layer and R_{Sf} is the resistance of the heavily doped semiconductor regions and their ohmic contacts. The R_{Sf} term is basically the same parameter as the R_S which occurs in the reverse bias model. The more abrupt the P^+N^- and N^-N^+ transitions are, the more closely R_{Sf} will equal R_S. R_{Sf} can be minimized by using heavily doped P^+ and N^+ regions, limiting their thickness to a minimum and by using low-resistance contacts.

For an abrupt-junction model PIN diode, the intrinsic region resistance, R_I, is given by:

$$R_I = \frac{W_1^2}{2 I_f \bar{\mu} \tau_L} \qquad (1\text{-}10)$$

where W_1 is the I-region width, I_f the DC forward current, $\bar{\mu}$ is the average carrier mobility and τ_L is the carrier lifetime in the intrinsic region. To minimize R_I, one needs high quality intrinsic layers in order to maximize $\bar{\mu}$ and τ_L. R_I increases as W_1^2. Since W_1 is directly related to the breakdown voltage, one should not use higher V_b diodes than necessary to maintain a low R_I. Equation 1-10 shows that R_I can always be made insignificant by increasing I_f. However, in order to minimize DC control power, to simplify diode driver designs, and to minimize switching speed, it is

desirable to have I_f as low as possible. By combining equations 1-9 and 1-10:

$$R_f = \frac{W_1^2}{2I_f\bar{\mu}\tau_L} + R_{sf} \qquad (1\text{-}11)$$

For a PIN diode, R_f decreases with increasing I_f to approach R_{sf} asymptotically. The variation of R_f with I_f can be used to make current controlled RF attenuators. For sufficiently large I_f, so that R_f is low, the forward-biased PIN diode can be used in series with a transmission line to pass microwave power or in shunt to block microwave power. For low-voltage PIN diodes, I_f = 10 mA is sufficient to have $R_f \approx R_{sf}$, while for high voltage PIN diodes an I_f of 150 to 200 mA is needed to have $R_f \approx R_{sf}$. Hines[3] has proposed a figure of merit for PIN diodes similar to the cutoff frequency figure of merit used for multiplier varactors. The Hines figure of merit, f_{cs}, is given by:

$$f_{cs} = \frac{1}{2\pi C_j \sqrt{R_f R_s}} \qquad (1\text{-}12)$$

To maximize f_{cs}, it is desirable to have C_j, R_f and R_s as low as possible. In practice, a tradeoff between C_j and the resistance values must be made to obtain optimum performance for a given switching or phase shifting application. For the case of $R_f \approx R_s$, Equation 1-12 reduces to the equation for cutoff frequency for a varactor diode.

The fundamental ability of the PIN diode to change from a low value of resistance under forward bias to a low loss capacitor under reverse bias, leads to a wide variety of RF switching, phase shifting and attenuating applications for PIN diodes.

1.6 TRANSIENT PROPERTIES

When a PIN diode in an equilibrium reverse-bias state is switched into the forward-bias state, the transient occurs very rapidly. Carrier injection begins almost immediately, and the carrier concentration in the intrinsic regions grows to an equilibrium value. A finite amount of charge must be transferred in order for the junction to reach its equilibrium forward-bias value. The speed of the transient depends primarily on the time constant of the PIN diode and bias network, with an almost negligible delay due to the diode's junction effects.

(3) M.E. Hines, "Fundamental Limitations in RF Switching and Phase Shifting Using Semiconductor Diodes", Proc. IEEE., Vol. 52, No. 6, June 1964.

The situation is different when a forward-biased diode in equilibrium is suddenly switched into reverse bias. The steady state final reverse current will be the device's leakage current (I_{rs}). However, immediately after switching the diode can support a high value of reverse current I_r from the charge that is stored in the I-region. To support a value of I_r, the carrier concentration slope adjusts itself to supply the current by diffusion from both edges of the I-region. The stored charge depletes itself by two mechanisms. The first is the charge removal caused by I_r, which results in regions depleted of charged carriers starting at each end of the I-region and growing towards the center. The second is the decay of the injected carriers by recombination in the I-region. This recombination proceeds with a time constant, τ_L, which is the average lifetime of a charge carrier in the I-region before it recombines.

Figure 1.6-1 shows a typical switching transient of a PIN diode when switched from a given I_f to a given I_r. The diode is supplying the reverse current I_r from its stored charge which has built up during forward bias. It is to be expected that this reverse current can only be supported for a finite amount of time before the charge is depleted and the diode goes to its equilibrium state of reverse voltage and reverse leakage current. The length of time the current I_r can be sustained is called the storage time (τ_S). Out of necessity, τ_S is a function of both I_f and I_r since the first parameter determines the amount of stored charge and the second determines its rate of removal. The specific relation is given by:

$$\text{erf}\left(\frac{\tau_S}{\tau_L}\right)^{1/2} = \frac{1}{1 + I_r/I_f} \qquad (1\text{-}13)$$

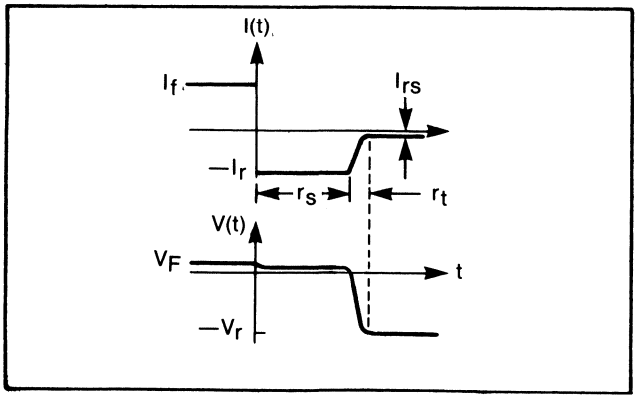


FIGURE 1.6-1 SWITCHING TRANSIENT OF A PIN DIODE

If a hole electron pair is created in the intrinsic layer, τ_L is the average time which elapses before the hole and electron are annihilated by recombination with an electron and hole respectively. For $I_r/I_f = 0.2$, τ_s is approximately equal to τ_L. By tradition, the standard method for measuring τ_L in diodes is to observe the switching transient for the case $I_r/I_f = 0.6$. Over the years the value of τ_s for $I_r/I_f = 0.6$ has become known as the carrier lifetime. The exact value of currents at which a measured τ_s is called τ_L is not critical, for the value should be regarded as a relative, rather than an exact parameter. In comparing diodes from one or more sources, one must be sure the test conditions for τ_L are the same in order to make a valid comparison of specifications.

After a time in the switching transient, an additional time to establish the equilibrium space-charge region is needed. This time interval is designated τ_t for transition time. Unless the PIN diode has very graded junctions or there are a large number of deep traps, τ_t is usually very much smaller than τ_s. Thus, τ_s is the dominant factor in determining the switching time from forward to reverse bias.

Because the transient is a function of both I_f and I_r, any real discussion of PIN diode switching time must include not only the PIN but also its driver. Drivers with high values of I_r or with spiked leading edges of their waveform are used to minimize reverse switching time. The fundamental lower limit is the transit time of the diode, or the minimum time it takes for a carrier to transit the I-region at maximum saturated velocity μ_s. The transit time is given by:

$$\text{Transit time} = \tau_t = \frac{W_1}{\mu_s} = \frac{W_1}{10^7}(\text{sec}) \qquad (1\text{-}14)$$

for W_1, the I-region width in centimeters. In this manner, the width of the I-region and/or the breakdown voltage determine the minimum speed with which the diode can be switched. Since high V_b diodes are needed to handle high RF power, it should be noted that the switching speed of a diode decreases as its power handling ability increases. Using conventional driver circuits, a typical 30 volt V_b PIN diode can be switched in 4 nanoseconds, while a typical 1500 V_b PIN diode can be switched in one microsecond.

1.7 POWER HANDLING

There are two factors which limit the amount of power a PIN diode can safely handle. The first and most common limitation is the maximum junction temperature at which the device can operate with full reliability. The second factor is the peak voltage that the device can be subjected to without causing damage to the junction.

The instantaneous voltage across a PIN diode junction is the algebraic sum of the DC bias voltage and the RF voltage. In the forward direction for slowly varying voltages, the diode will start to rectify to prevent high voltages and electric fields from occuring across the junction. For rapidly varying voltages, a voltage as high as $V_{RF_{peak}} - V_{bias}$ can be impressed on the diode without causing conduction. However, in the reverse direction, the maximum instantaneous reverse voltage which may be applied is

$$V_{max} = V_{RF_{peak}} + V_{bias} \qquad (1\text{-}15)$$

where V_{bias} is the DC reverse bias impressed on the diode. If V_{max} exceeds the breakdown voltage, the PIN diode will go into avalanche breakdown. For PIN diodes, the avalanche breakdown consists of high current density filaments since the PIN diode often exhibits DC negative resistance in the avalanche region. The temperature in the high current density filaments can easily reach levels which are descructive to the silicon, thus forming molten channels across the junction and permanently destroying it. The maximum value of V_{max} which can be sustained without risk of avalanche breakdown is a value just below V_b. Under this condition, however, there is no safety margin and it should not be used for reliable designs. White[4] has proposed a very conservative limit for V_{max} of $V_b/2$. A circuit designer must choose a relationship between V_{max} and V_b that he feels represents an acceptable margin of safety for each particular application.

The junction temperature of a PIN diode is determined by the ambient temperature of the circuit and the power dissipated within the diode. The dissipated power may be pulsed or CW. In either case, the junction temperature must be maintained below a maximum value. The specific junction temperature that is reached in a given application determines the MTBF of the diode for reliability purposes. This subject will be discussed in detail in Chapter 7. A temperature of 200°C is recommended as the maximum safe operating temperature of the junction.

(4) White, op. cit.

device physics of PIN diodes

10

The major parameter for determining junction temperature for CW power dissipation is θ_{jc}, the total thermal resistance in °C/watt. For a given power dissipated (P_d) the junction temperature (T_j) is given by:

$$T_j = T_a + P_d \theta_{jc} \quad (1\text{-}16)$$

where T_a is the ambient temperature. The value of θ_{jc} is determined by the physical volume of the active junction, the thickness and size of the diode substrate and the material and geometry of the package. Since most glass packages use long kovar leads, low-capacitance, small-area diode chips in glass packages have the highest values of θ_{jc}, typically around 600°C/watt. Large-area, high-capacitance chips mounted directly on copper heat sinks have extremely low values of θ_{jc}, typically 5°C/watt or less.

For the junction-region thermal resistance (θ_j) the following approximate expression is valid:

$$\theta_j = \frac{W_1}{K_{th} A} \quad (1\text{-}17)$$

where K_{th} is the thermal conductivity of silicon (0.80 watts/cm°C) and A is the junction area. As before, W_1 is the width of the I-layer. Note that in Equation 1-17, θ_j is the I-region thermal resistance only. The resistance that must be used in Equation 1-16 is the total thermal resistance θ_{jc} which consists of the sum of Equation 1-17 plus the thermal resistances of the layers and interfaces between the active region and the circuit heat sink.

For considering pulsed heating of the diode it is convenient to define a parameter called the thermal time constant (τ_{th}) of the active region. τ_{th} is analogous to the RC time constant of an electrical circuit of a resistor and capacitor in series and is given by:

$$\tau_{th} = (\theta_j)(HC) \quad (1\text{-}18)$$

where HC is the thermal capacity of the active region. Considering the geometry of the active region, HC may be expressed as:

$$HC = c_p \varrho V = c_p \varrho W_1 A \quad (1\text{-}19)$$

where c_p is the specific heat of silicon (0.760 joule/g°C), ϱ is the density of silicon (2.42 g/cm²) and V is the volume of the active region. Combining Equations 1-17, 1-18 and 1-19, τ_{th} may be expressed as:

$$\tau_{th} = \frac{c_p W_1^2 \varrho}{K_{th}} \quad (1\text{-}20)$$

Notice that for the time constant of the active region, the area has cancelled out and τ_{th} is independent of device area and depends only on I-layer width squared. τ_{th} is the time constant with which the active region approaches its equilibrium temperature, without any consideration for the temperature distribution in the rest of the chip, package and heat sink configuration.

For pulse widths of 0.25 τ_{th} or less, the active area of the device must absorb all the thermal energy since there is no time for it to spread into the surrounding material. For such short pulses the amount of energy dissipated in the diode is:

$$\text{Energy} = P_d \Delta t \text{ (joules)} \quad (1\text{-}21)$$

where P_d is the power dissipated and Δt is the pulse duration. Since all the energy serves to heat the small active region, it can also be stated that:

$$\text{Energy} = (HC)\,\Delta\,T \text{ (joules)} \quad (1\text{-}22)$$

where ΔT is the temperature rise of the junction. Combining these two relations gives the following expression for the short pulse temperature rise:

$$\Delta T = \frac{(P_d)(\Delta t)}{HC} (°C) \quad (1\text{-}23)$$

The pulse length over which Equation 1-23 is valid varies from 50 nsec for small low voltage PINs to 75μsec for the highest voltage PINs.

For time intervals from approximately 0.25 τ_{th} to 3 or more times τ_{th}, the PIN diode junction temperature follows an exponential curve given by:

$$T_j = T_a + P_d \theta_j (1 - e^{-t/\tau_{th}}) \quad (1\text{-}24)$$

Note that Equation 1-24 contains θ_j, the junction thermal resistance and not θ_{jc} the total thermal resistance. For cooling between pulses, the junction temperature follows an exponential decay with the same time constant τ_{th}.

For successively longer pulsewidths, the thermal model must be expanded to account for the heat spreading into the substrate and package. As the pulsewidth increases, successive time intervals can be modeled by an appropriate thermal time constant until, finally, the equilibrium (T_j) governed by the total thermal resistance (θ_{jc}) is reached.

11

PIN diode switch design book

2.1 DISCUSSION

The purpose of this chapter is to analyze the insertion loss and isolation performance of numerous switch types. Throughout this chapter, the following basic assumptions are made:

(1) When more than one PIN is required in a switch, all devices are assumed to be similar.
(2) In all cases, it is assumed that no diode parasitics are encountered.
(3) The same curves will be valid for packaged PIN diodes if the parasitics C_p (packaged capacitance) and L_s (lead inductance) are tuned out. (See Chapter 6.)
(4) The frequency range under consideration is from 10 MHz to 20 GHz. Plots are presented over the entire frequency range for each switch type unless electrical performance decays to a point where switch parameters are unreasonable.
(5) For these analyses, the equivalent circuits of the PIN diode for each bias mode are assumed to be as shown in Figure 2.1-1.
(6) All transmission lines are assumed to be lossless.
(7) The curves apply to a characteristic impedance of 50 ohms except where otherwise specified.

Also discussed in this chapter is the power distribution in series, parallel and combination circuits. Design curves indicating required breakdown voltage and thermal considerations are presented. In Section 2.12 the performance of three multi-throw switches using packaged diodes **without parasitics being tuned out** will be discussed.

In order to avoid confusion, a schematic drawing of each switch type discussed in this book, in each operational mode is included in Figure 2.1-2. In each schematic, a matched constant voltage generator is shown attached to the circuit. Each circuit is terminated in a matched load. External biasing of each chip or set of chips is to be in accordance with Figure 2.1-1. For future reference, Figures 2.1-3 and 2.1-4, showing capacitance and inductive reactance as a function of frequency, are included.

In addition to the generalized curves of this chapter, the actual performance of 16 different Microwave Associates PIN chip types is described graphically in Chapter 10. The performance of each chip type is analyzed in a series of 17 different switch designs where applicable.

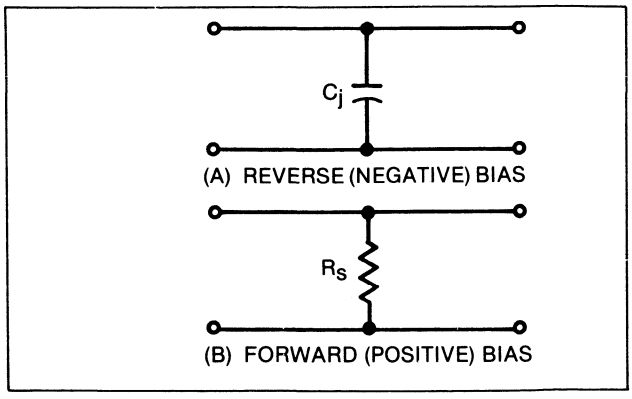


FIGURE 2.1-1 EQUIVALENT PIN DIODE CIRCUITS

FIGURE 2.1-2 PIN SWITCH SCHEMATICS

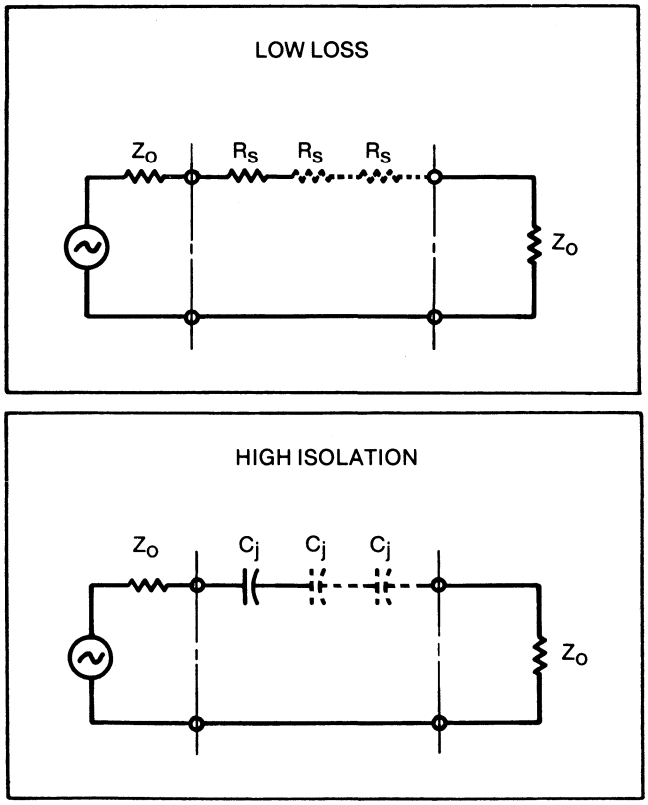


FIGURE 2.1-2a 1, 2, 3 DIODE SERIES MOUNTED SPST SWITCH

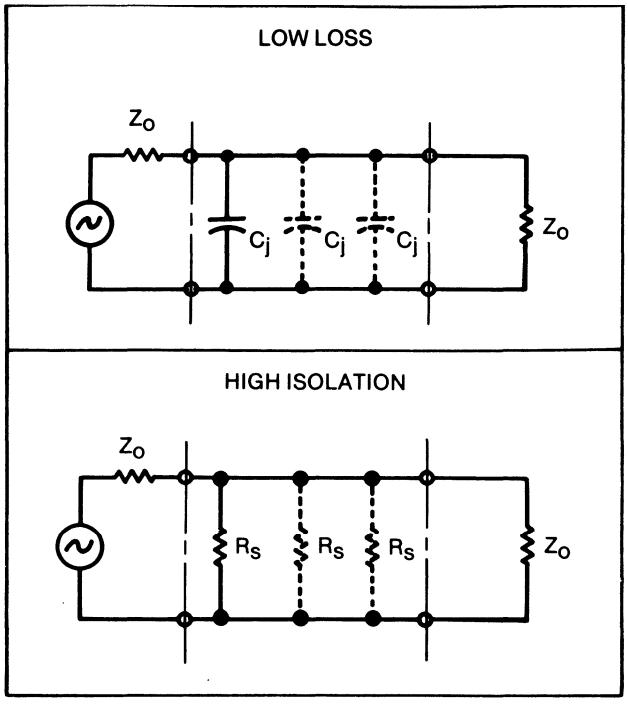


FIGURE 2.1-2b 1, 2, 3 DIODE SHUNT MOUNTED SPST SWITCH

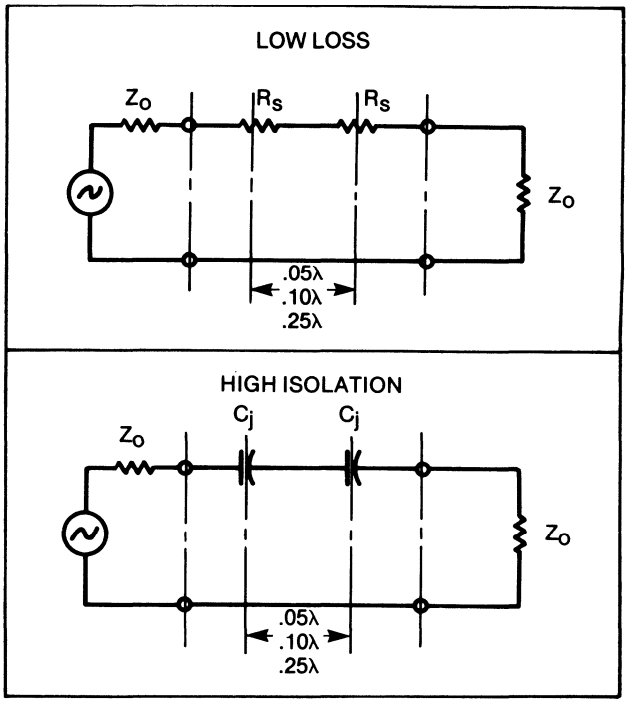


FIGURE 2.1-2d 2 ITERATED SERIES DIODES — SPST SWITCH — .05λ, .10λ, .25λ APART

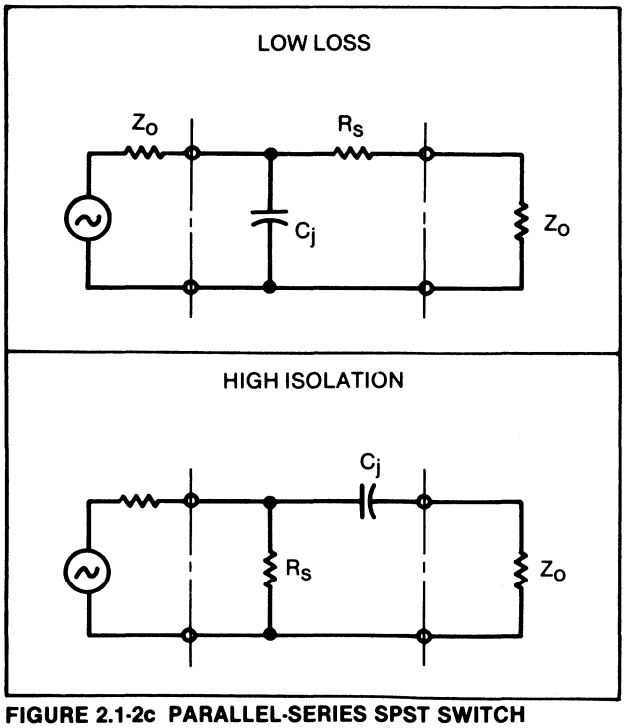


FIGURE 2.1-2c PARALLEL-SERIES SPST SWITCH

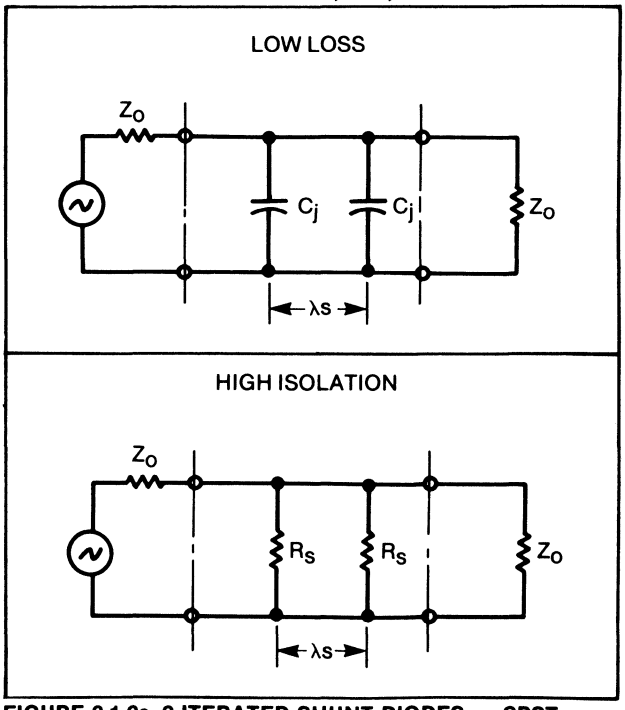


FIGURE 2.1-2e 2 ITERATED SHUNT DIODES — SPST SWITCH

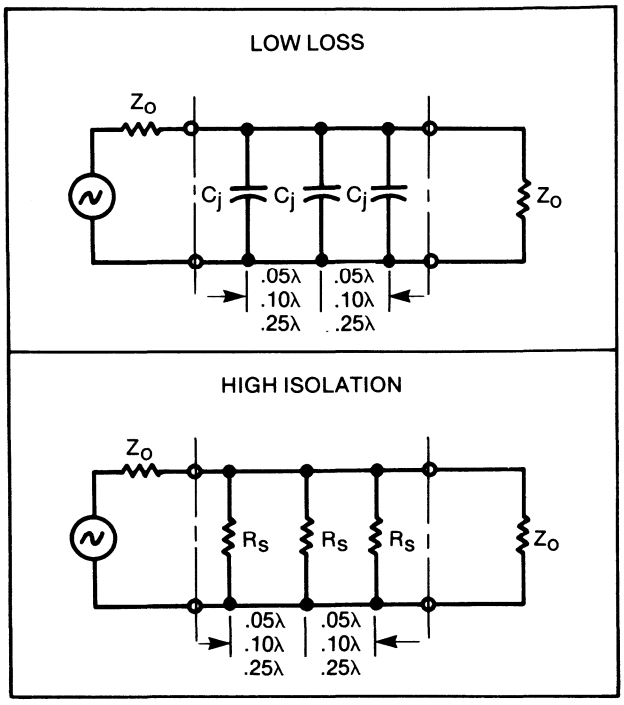


FIGURE 2.1-2f 3 ITERATED SHUNT DIODES — SPST SWITCH — .05λ, .10λ, .25λ APART

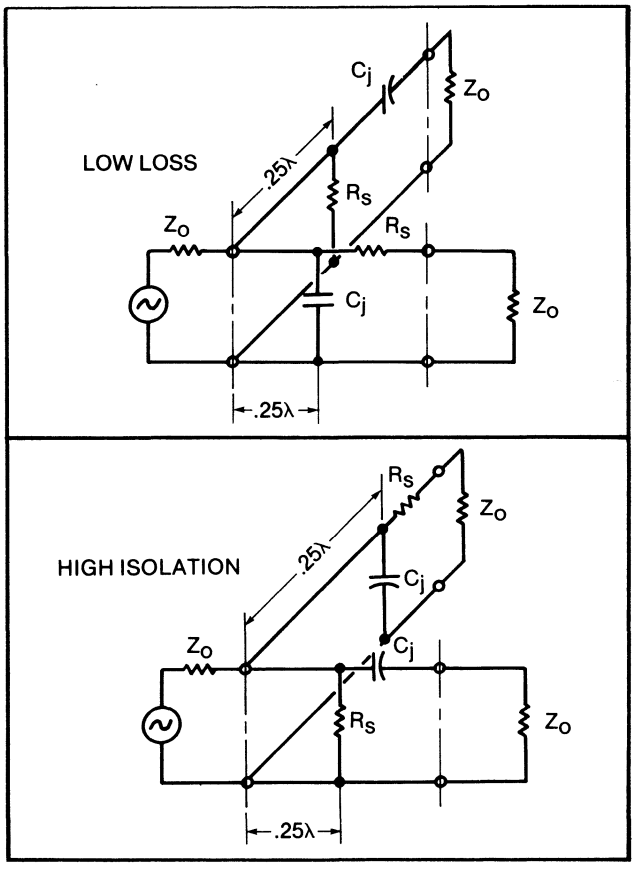


FIGURE 2.1-2g PARALLEL-SERIES SPDT SWITCH

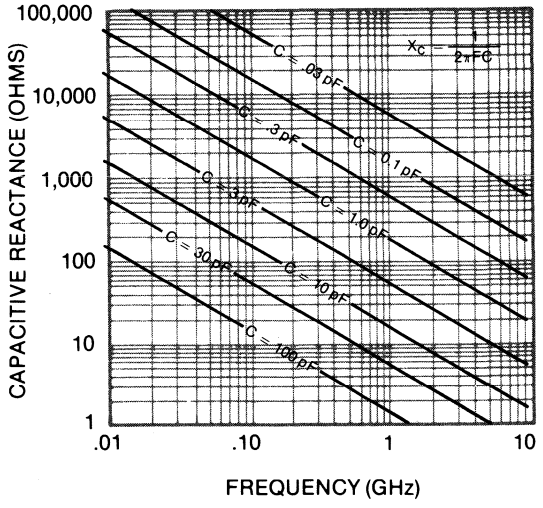


FIGURE 2.1-3 CAPACITIVE REACTANCE AS A FUNCTION OF FREQUENCY AND CAPACITANCE

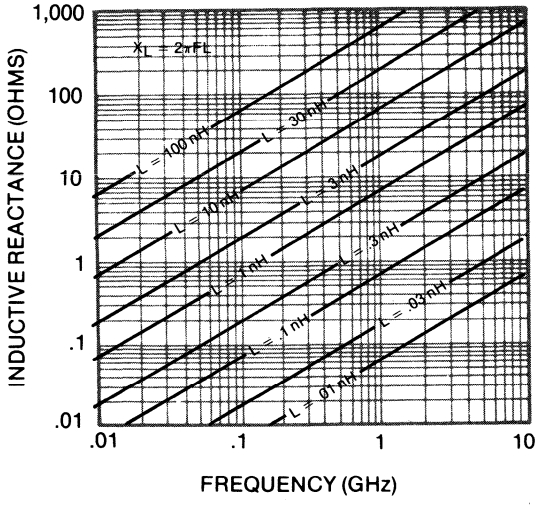


FIGURE 2.1-4 INDUCTIVE REACTANCE AS A FUNCTION OF FREQUENCY AND INDUCTANCE

2.2 SPST SERIES SWITCH

A switch with one of the simplest methods of mounting (depending on the specific transmission line configuration) is a single or multiple diode series switch, as shown in Figure 2.1-2a. This switch style features reasonable isolation and insertion loss performance at a relatively low function cost. Both beam-lead and axial-lead glass or pronged ceramic packages lend themselves quite easily to this mounting technique. For this particular analysis, the series mounted devices are assumed to have no electrical spacing between them.

Figure 2.2-1a shows a plot of insertion loss vs R_S at several different values of Z_O. For any value of R_S, lowering the characteristic impedance results in an improved insertion loss. Theoretically, insertion loss is a frequency independent parameter for this type of switch. Figure 2.2-1b indicates the isolation performance of the series switch as a function of frequency and reverse bias capacitance. It becomes evident that a considerable isolation advantage can be realized at the cost of only a slight increase in insertion loss if additional series diodes are added to the structure. However, isolation in a series switch is

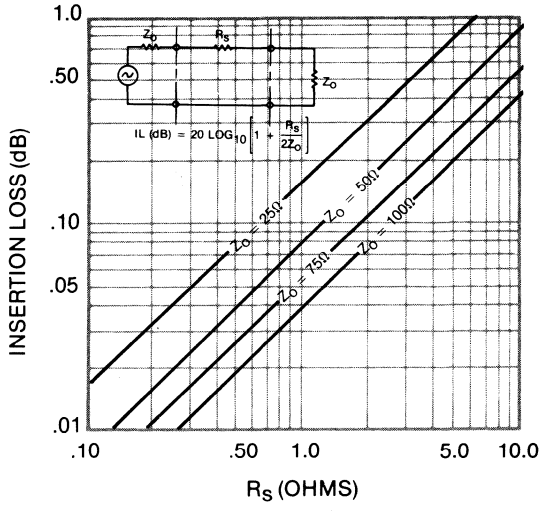


FIGURE 2.2-1a INSERTION LOSS VS R_S FOR A SINGLE DIODE SPST SERIES PIN SWITCH

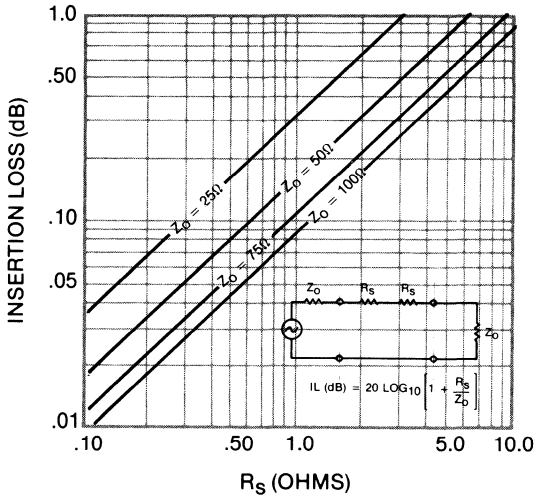


FIGURE 2.2-1c INSERTION LOSS VS R_S FOR A TWO DIODE SPST SERIES PIN SWITCH

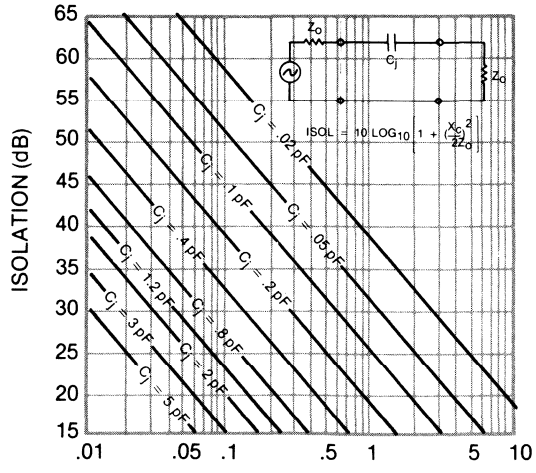


FIGURE 2.2-1b ISOLATION VS FREQUENCY FOR A SINGLE DIODE SPST SERIES PIN SWITCH

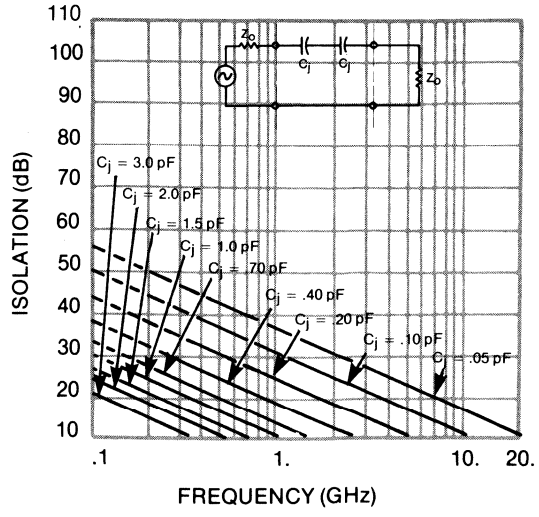


FIGURE 2.2-1d ISOLATION VS FREQUENCY

extremely frequency-dependent. Figures 2.2-1c and 2.2-1d show the insertion loss and isolation performance of two series diodes with equal values of C_j and R_S.

2.3 SHUNT SWITCHES

Figure 2.1-2b shows a one, two or three-diode configuration in shunt with the transmission line with no electrical spacing between devices. Because the beam-lead structure (M/A case style 129) definitely does not lend itself to this type of switch or, in fact,

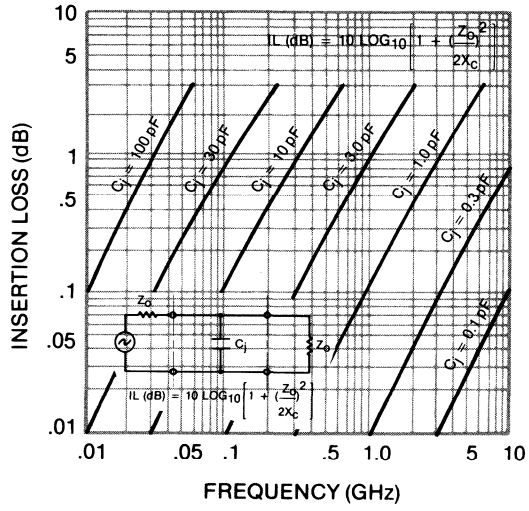


FIGURE 2.3-1a INSERTION LOSS VS FREQUENCY FOR A SINGLE DIODE SPST SHUNT PIN SWITCH

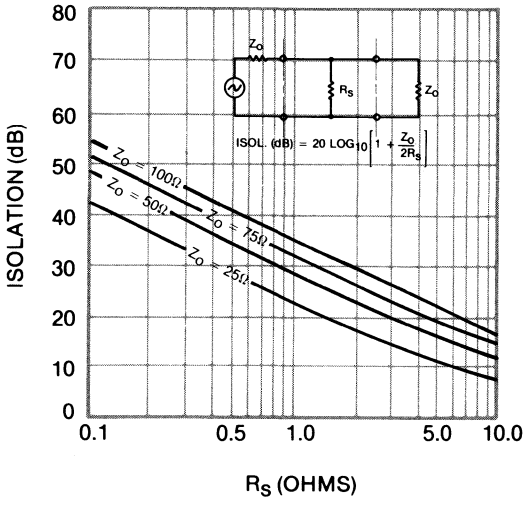


FIGURE 2.3-1b ISOLATION VS R_S FOR A SINGLE DIODE SPST SHUNT PIN SWITCH

shunt mounting in any switch type, potential electrical performance of the MA-4P101-129 and MA-4P102 will not be evaluated for any shunt configurations. Figures 2.3-1a and 2.3-1b show that, unlike the series mounted switch, the shunt or parallel switch features quite low, frequency-dependent insertion loss and a medium (and theoretically contant) isolation vs frequency characteristic.

Depending upon desired performance, the number of shunt diodes to be used may be determined by function cost. Increasing the number of shunt diodes will improve the isolation while increasing the insertion loss. However, it is often more economical to use two lower quality (and lower-priced) diodes in a switch to attain acceptable electrical performance than it is to use one diode with extremely high quality parameters and moderate pricing.

2.4 PARALLEL-SERIES SWITCHES

Combination switches can often offer substantial advantages over straight multi-diode series or parallel circuits. The parallel-series configuration shown in Figure 2.1-2c illustrates these advantages. Depending on the actual diode parameters, a parallel-series combination can offer both higher isolation than a two-diode parallel switch with the same diode types, and lower insertion loss than a two-diode series switch. The SPST parallel-series design curves of Figure 2.4-1 illustrate this. Isolation is always a function of frequency in this type of switch. However, there is a critical frequency below which insertion loss is quite low and almost frequency independent. This is shown in Figure 2.4-2, plotted as a function of junction capacitance.

Whether the parallel or series diode appears first in the array makes no difference in isolation and insertion loss for a SPST switch. However, the relative order is a prime consideration with a multiple throw switch. If the devices are mounted right at the junction in a multi-throw switch, the series diodes must be ahead of the parallel devices, so that the "OFF" arms present a high impedance to the junction. If the devices are to be spaced $\lambda/4$ from the switch juncture, the shunt diodes must be mounted ahead of the series devices, so that the "OFF" arms can reflect the same high impedance back to the junction.

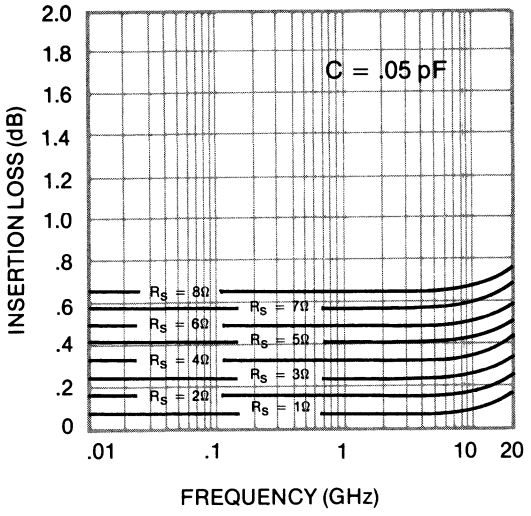


FIGURE 2.4-1a INSERTION LOSS VS FREQUENCY

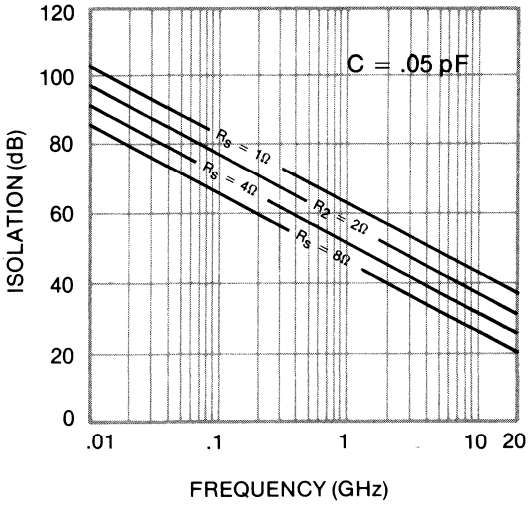


FIGURE 2.4-1b ISOLATION VS FREQUENCY

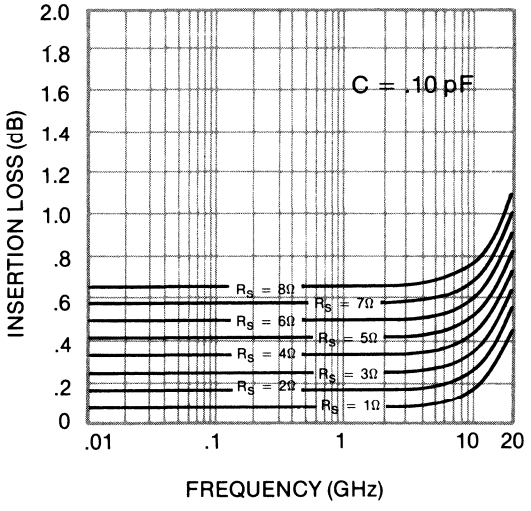


FIGURE 2.4-1c INSERTION LOSS VS FREQUENCY

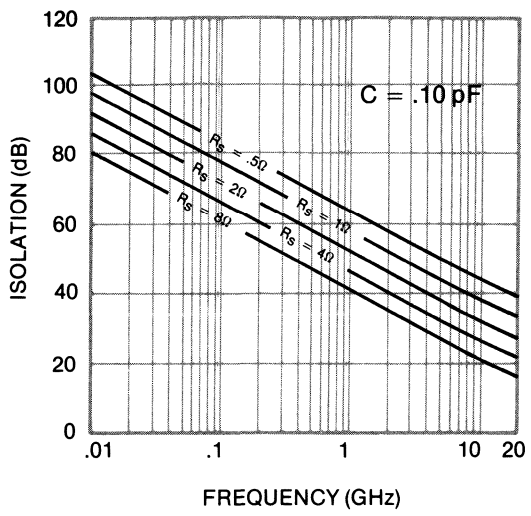


FIGURE 2.4-1d ISOLATION VS FREQUENCY

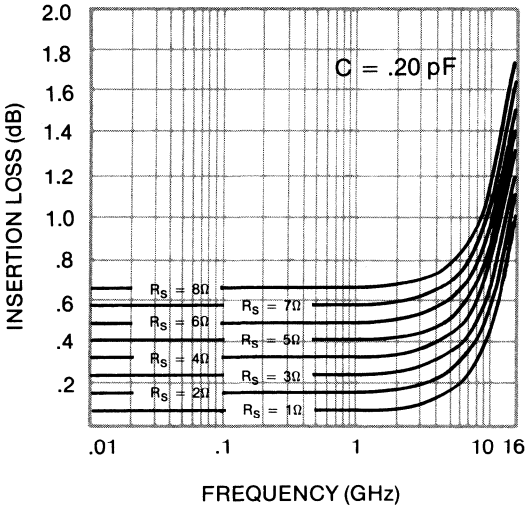


FIGURE 2.4-1e INSERTION LOSS VS FREQUENCY

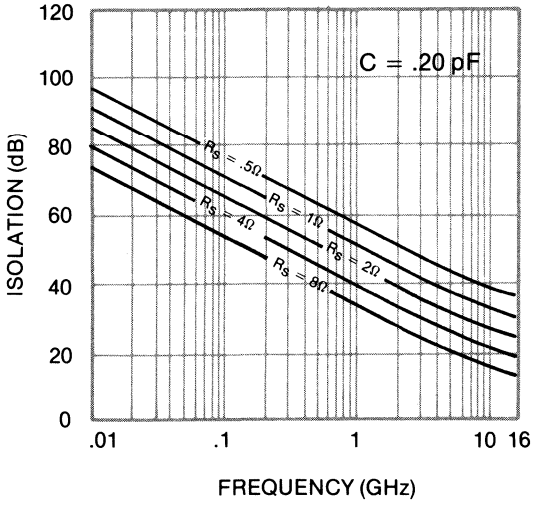


FIGURE 2.4-1f ISOLATION VS FREQUENCY

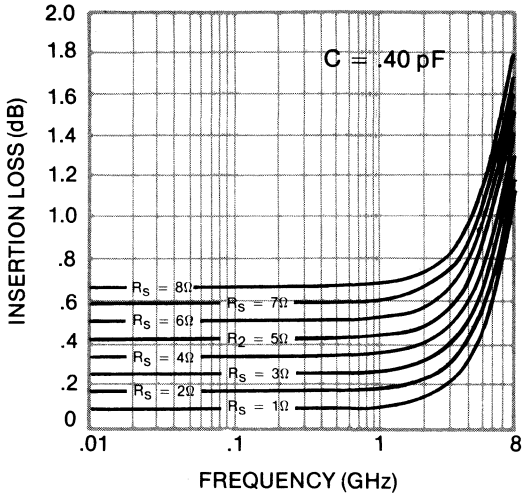


FIGURE 2.4-1g INSERTION LOSS VS FREQUENCY

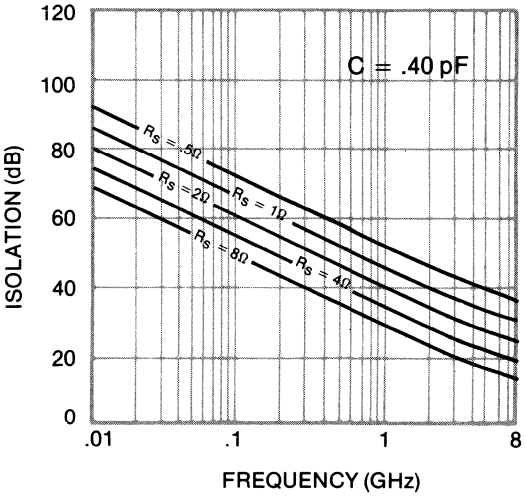


FIGURE 2.4-1h ISOLATION VS FREQUENCY

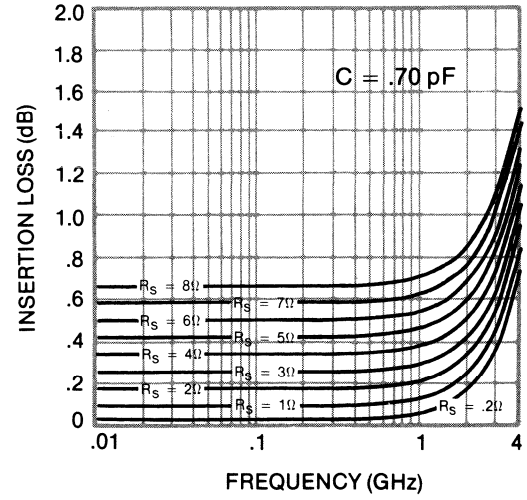


FIGURE 2.4-1i INSERTION LOSS VS FREQUENCY

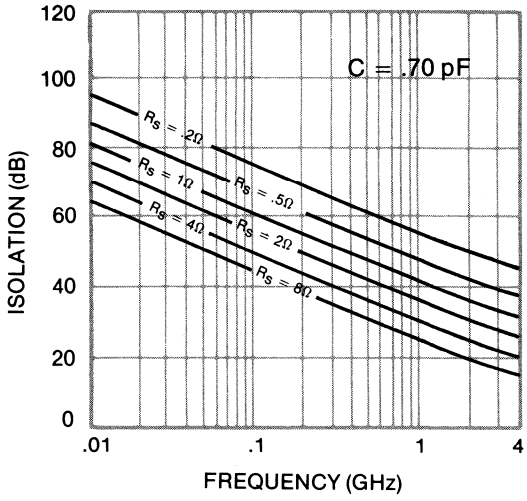


FIGURE 2.4-1j ISOLATION VS FREQUENCY

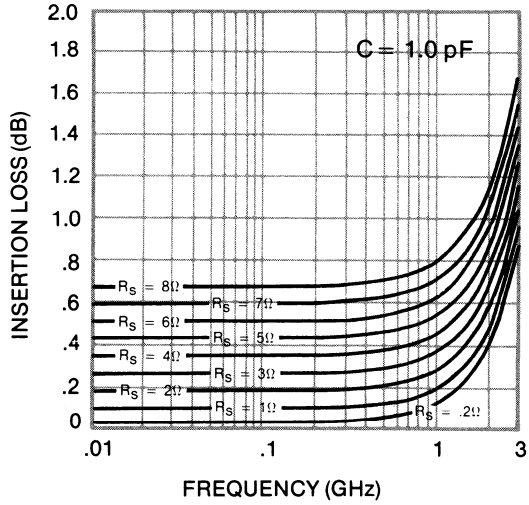


FIGURE 2.4-1k INSERTION LOSS VS FREQUENCY

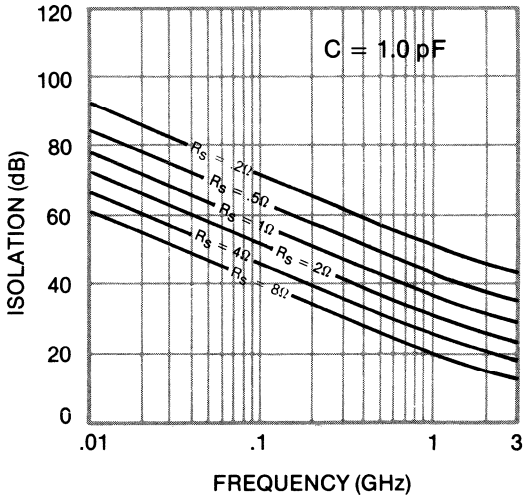


FIGURE 2.4-1m ISOLATION VS FREQUENCY

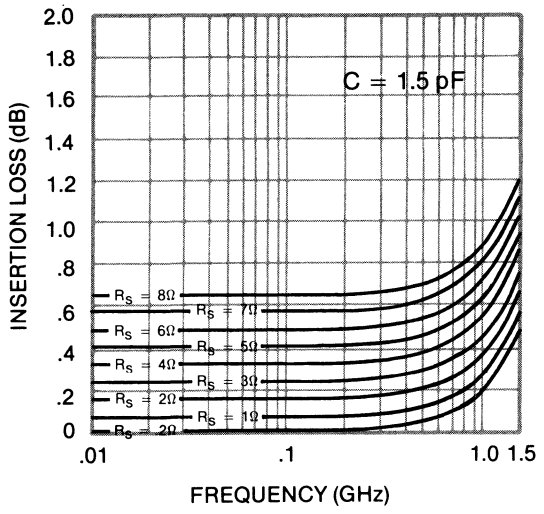


FIGURE 2.4-1n INSERTION LOSS VS FREQUENCY

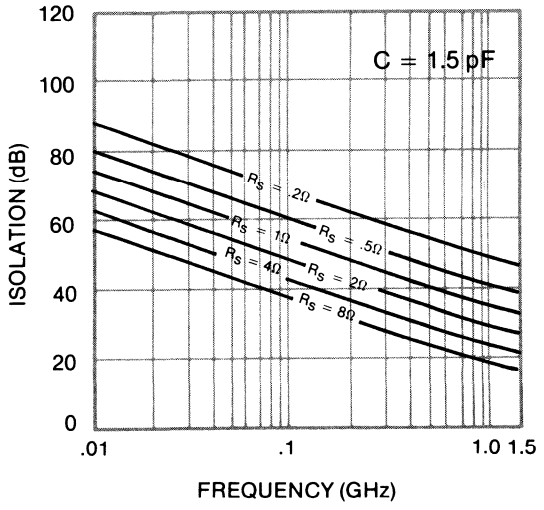


FIGURE 2.4-1o ISOLATION VS FREQUENCY

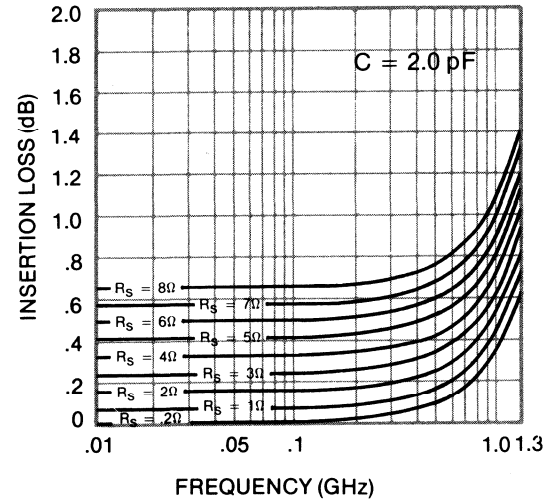


FIGURE 2.4-1p INSERTION LOSS VS FREQUENCY

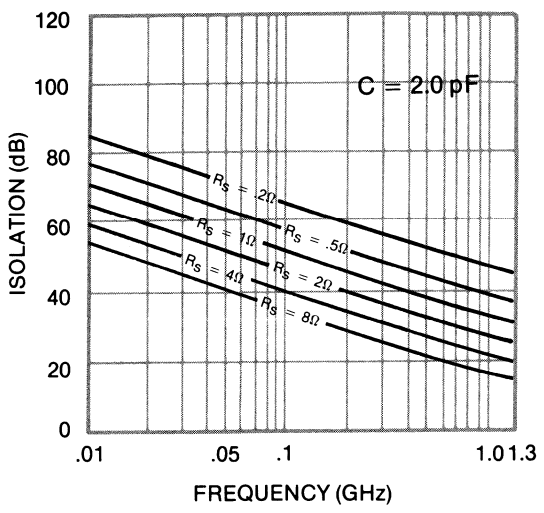


FIGURE 2.4-1q ISOLATION VS FREQUENCY

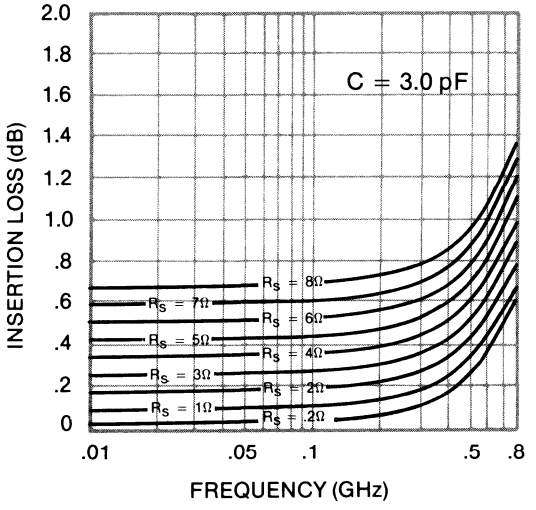


FIGURE 2.4-1r INSERTION LOSS VS FREQUENCY

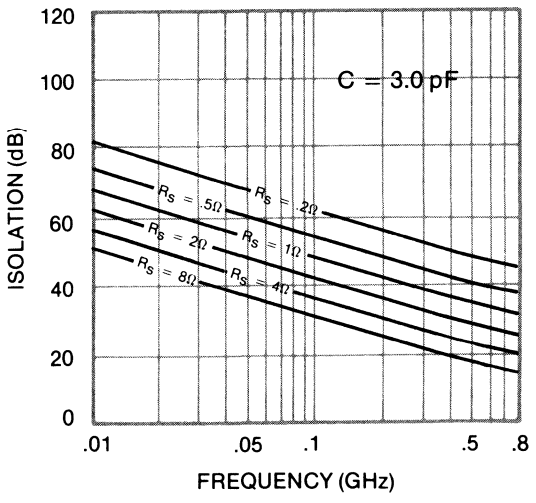


FIGURE 2.4-1s ISOLATION VS FREQUENCY

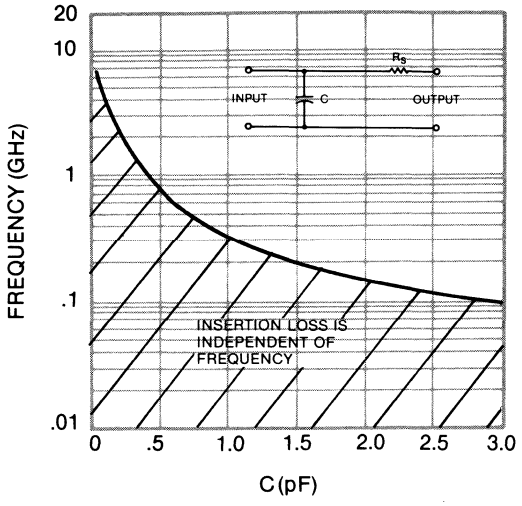


FIGURE 2.4-2 PARALLEL-SERIES SWITCH-FREQUENCY AT WHICH INSERTION LOSS BECOMES FREQUENCY INDEPENDENT

2.5 DIODE ITERATIONS

An iteration can be described as a "repeat performance". Technically, two similar series or shunt diodes placed next to each other (zero electrical space) form an iterated pair. However, for RF switches, diode iterations generally refer to diodes that are spaced apart by some electrical distance, usually to enhance electrical parameters. Usually these iterations are parallel in nature and $\lambda/4$ in spacing. Sections 2.5, 2.6, 2.7 and 2.8 will explore not only shunt iterations at $\lambda/4$ but also both series and shunt iterations at various spacings and will indicate the advantages and drawbacks to each approach.

The design curves will show that at some lower frequencies where $\lambda/4$ spacing is not feasible because of extremely large wavelengths, very small electrical separations result in greatly improved performance. In many applications, even large electrical separation when used with dielectrically loaded transmission lines, are quite practical. As a guide to practicality, Figure 2.5-1 provides a series of curves plotting wavelength vs frequency for several single-medium TEM transmission lines. A multi-medium transmission line, such as microstrip, requires a modification of the dielectric constant to an effective and relative value. This effective value can be obtained from Figure 2.5-2. Then the effective wavelength can be calculated from:

$$\lambda_E \text{ (inches)} = \frac{3(10)^{10}}{(\sqrt{\epsilon_R})\,(F)\,(2.54)}$$

where λ_E is the effective wavelength, ϵ_R is the effective dielectric constant relative to air and F is the frequency.

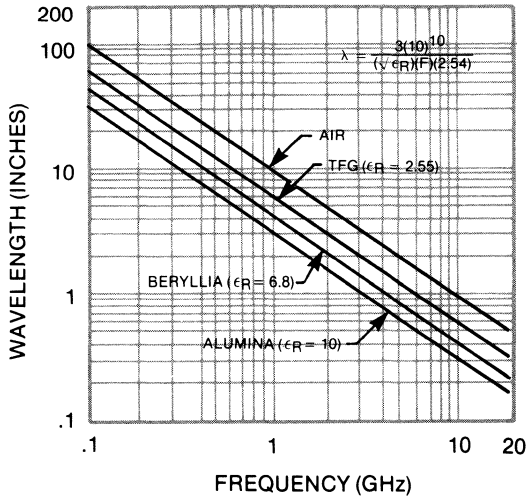


FIGURE 2.5-1 WAVELENGTH VS FREQUENCY FOR SINGLE MEDIUM TEM TRANSMISSION LINES

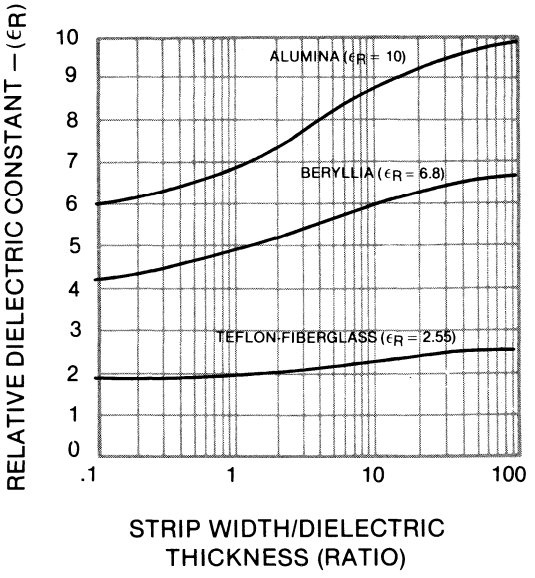


FIGURE 2.5-2 CORRECTION FOR DIELECTRIC CONSTANT IN MICROSTRIP TRANSMISSION LINE

2.6 SPST SERIES ITERATED DIODE SWITCHES

The broadest bandwidths for low-power untuned switches can be achieved with beam-lead PIN diodes (MA-4P101 and MA-4P102-129). These extremely low parasitic devices feature small physical size, low capacitance and relatively low values of forward bias series resistance. Because of their construction they are suited for series mounting only. In fact, in many applications, a series configuration is the only structure that can be tolerated with any diode model. Although single series diode performance does have some limitations, multiple series diode arrays, especially with appropriate electrical spacings, can provide excellent electrical characteristics when used as RF switches. To determine what is appropriate, one must analyze the frequency of operation and select a transmission medium before a rational choice of PIN devices and spacing can be made. The equivalent circuit for both operational modes of a two-diode series-iterated SPST switch is shown in Figure 2.1-2d.

Because of the extreme size of a wavelength at very low frequencies, design curves for the two-diode iterated switch shown in Figure 2.6-1 have all been limited to frequencies at or above 100 MHz. Perhaps the most interesting aspect of the two-diode series iteration is the family of insertion loss curves shown in Figure 2.6-1a. The insertion loss for any pair of series diodes regardless of spacing is essentially flat, and is under 1.4 dB for pairs of diodes with series resistance values as high as 8 ohms. The greatest deviation from constant insertion loss occurs at the highest R_S value and shows only a 0.1 dB change between 0 and λ/2 spacing, peaking at λ/4. In fact, diodes having R_S values lower than 3 ohms offer essentially the same loss regardless of spacing. The isolation of two series-iterated diodes separated by a spacing of λ/4 is double that of a single series device, plus 6 dB.

The isolation performance of series-iterated diodes spaced at λ/4, λ/10 and λ/20 is shown in Figures 2.6-1b, 2.6-1c and 2.6-1d. It is important to compare these design curves with Figure 2.2-1d which shows the isolation provided by two series diodes of equal R_S and no electrical spacing. As a typical example, at 1 GHz, two series .05 pF diodes spaced λ/4 apart offer an 83% increase in isolation over the same diodes with zero spacing. Additionally, these diodes, even when separated by as little as λ/20, still offer an isolation advantage of over 55% when compared to a two-diode series switch having no electrical spacing. All this advantage and no increase in insertion loss! There is always, however, one spacing that is better (isolation is highest) than all the rest. At low values of capacitance this point is decidedly at λ/4, but as capacitance increases, more and more phase shift is encountered due to the PIN diodes. As a result, the optimum spacing for maximum isolation, although relatively broad, shifts significantly with increasing frequency. As a typical example, Figure 2.6-1e shows both the shift in optimum spacing and changing isolation magnitude as a function of frequency for two 1.5 pF diodes series-iterated. As shown, at a frequency as low as 0.5 GHz, not only is the optimum spacing at about .19λ but also at a spacing of about .45λ

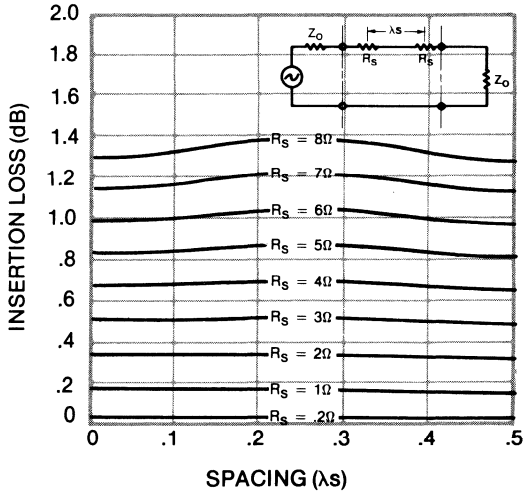


FIGURE 2.6-1a TWO SERIES-ITERATED DIODES — INSERTION LOSS VS SPACING

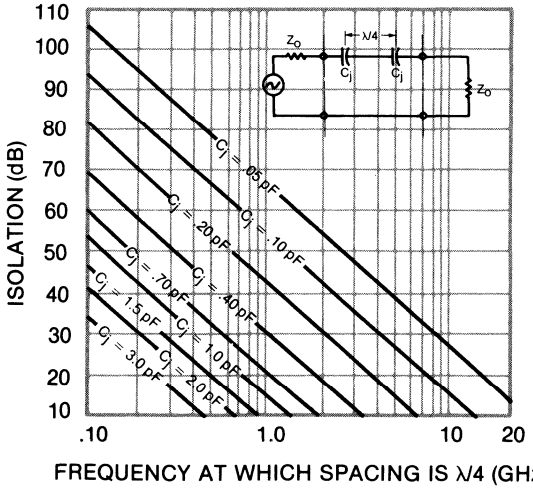


FIGURE 2.6-1b TWO SERIES-ITERATED DIODES — λ/4 APART — ISOLATION VS FREQUENCY

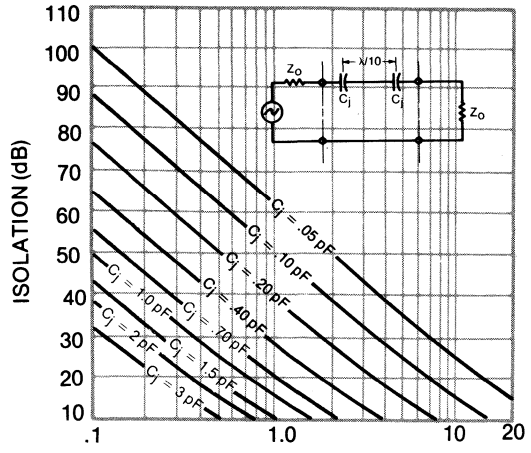


FIGURE 2.6-1c TWO SERIES-ITERATED DIODES — λ/10 APART — ISOLATION VS FREQUENCY

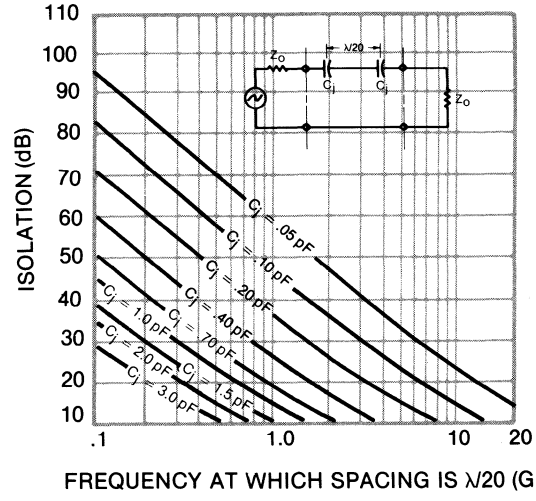


FIGURE 2.6-1d TWO SERIES-ITERATED DIODES — λ/20 APART — ISOLATION VS FREQUENCY

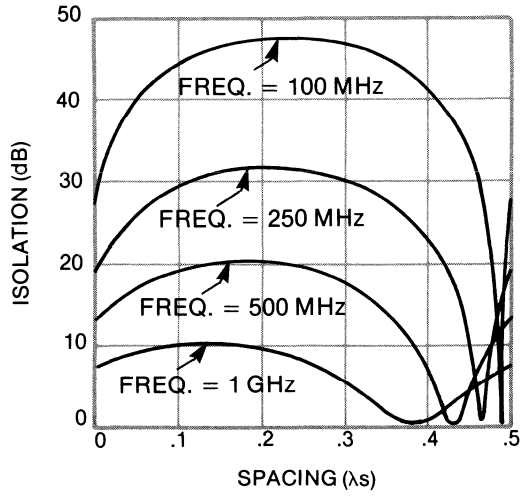


FIGURE 2.6-1e TWO 1.5 pF SERIES-ITERATED CHIPS — ISOLATION VS SPACING

the isolation drops to zero. This effect will be illustrated graphically over a much wider frequency range when the design curves using the beam-lead diodes MA-4P101 and MA-4P102 are presented, in Chapter 10.

2.7 TWO-DIODE SHUNT-ITERATED SPST SWITCH

Figure 2.1-2e shows the equivalent circuits for the pass and reject modes in a two-diode shunt-iterated SPST switch. Unlike the series-iterated switch, the shunt-iterated version features isolation performance that is theoretically frequency independent. Figure 2.7-1 shows a very useful family of design curves which plot switch isolation as a function of both device spacing and varying R_S. Here the advantage of electrically spacing two shunt diodes becomes immediately obvious. So broad is this family of curves that even a slight electrical spacing between two shunt devices provides a large increase in switch isolation. Optimum isolation for any device R_S occurs at a spacing of λ/4. As frequency increases, shunt-iterated diodes exhibit an increased insertion loss. Figure 2.7-2 uses, as an example, a pair of diodes with C_j = .7 pF at various electrical spacings. It will be noticed that the minimum value of insertion loss is always zero, but due to phase shifting, the diode spacing for this minimum loss always decreases as frequency increases. This change is more dramatic and the point of minimum loss becomes more and more selective as C_j increases. In the example shown, the optimum spacing for minimum insertion loss at 100 MHz is λ/4 but at 10 GHz the optimum spacing is only .118λ. If, in an effort to get maximum loss in the reject mode, λ/4 spacing were to be used with these two devices at 10 GHz, the resulting insertion loss would be 8.5 dB.

The design curves of Figure 2.7-3 emphasize the effect that frequency has on optimum spacing for minimum insertion loss for a variety of values of C_j. The design procedure, then, for a two-diode iterated switch should consist of three steps:

(1) In order to obtain minimum insertion loss, use Figure 2.7-3 to determine the optimum spacing needed for the two PIN diodes selected. (Diode selection as a function of power dissipation and frequency will be covered later in this chapter.)
(2) Refer to Figure 2.5-1 to determine if this is a practical spacing for the design frequency.
(3) Refer to the design curves of Figure 2.7-1 to determine the value of isolation that can be obtained with the spacing chosen in step 1.

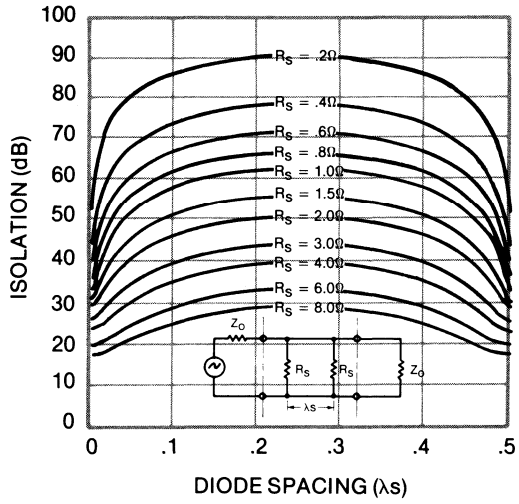


FIGURE 2.7-1 TWO SHUNT-ITERATED DIODES — ISOLATION VS SPACING

FIGURES 2.7-2 TWO SHUNT-ITERATED DIODES (C_j = 0.7 pF) — INSERTION LOSS VS SPACING

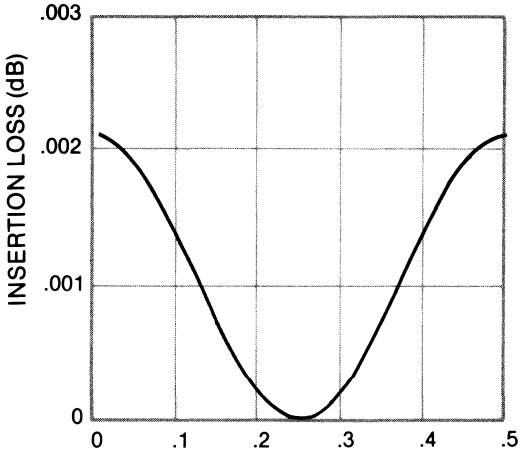


FIGURE 2.7-2a FREQUENCY = 0.1 GHz

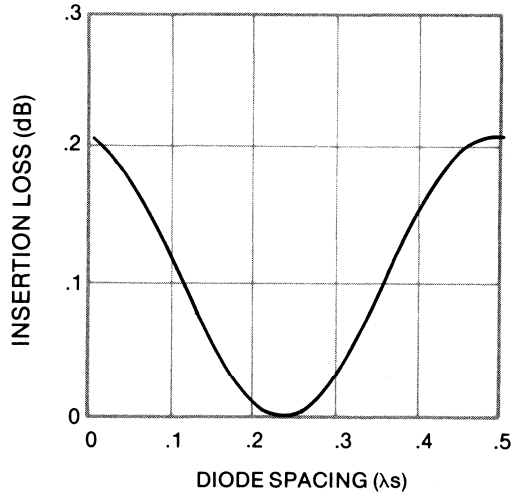


FIGURE 2.7-2b FREQUENCY = 1.0 GHz

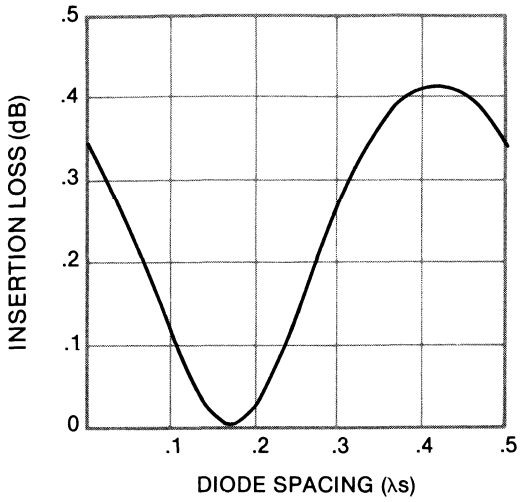


FIGURE 2.7-2c FREQUENCY = 5.0 GHz

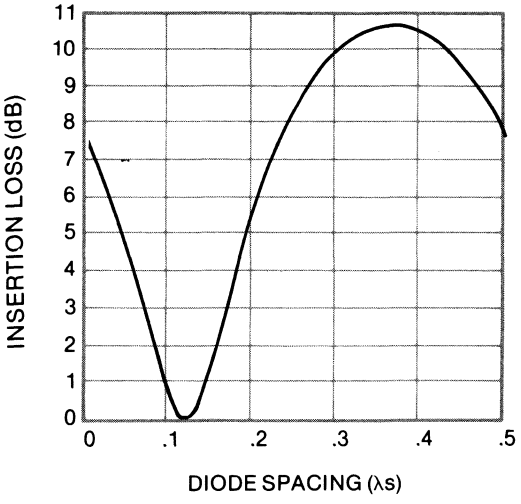


FIGURE 2.7-2d FREQUENCY = 10.0 GHz

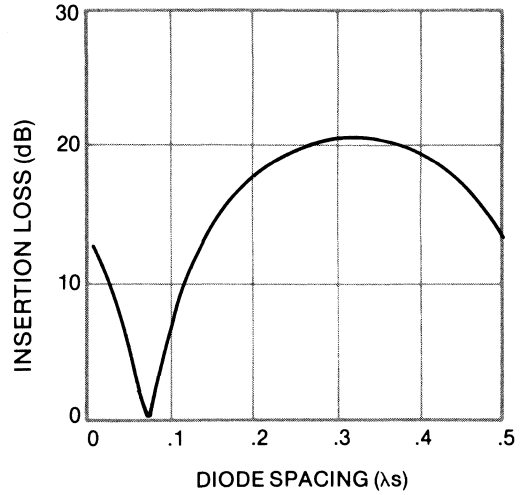


FIGURE 2.7-2e FREQUENCY = 20 GHz

If the values obtained from this procedure are within the design criteria, proceed with the mechanical design of the switch. If not, select from the other SPST switch options, or select another pair of diodes.

No attempt has been made to predict the bandwidth of any of the design procedures described herein. Whenever electrical spacing is discussed and design curves presented, the spacing has been generalized to include any frequency.

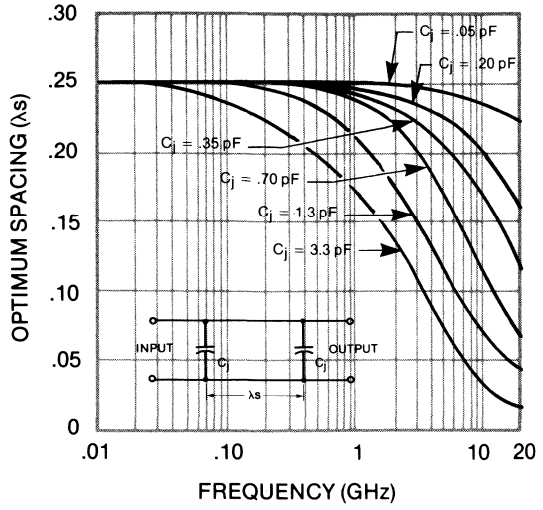


FIGURE 2.7-3 OPTIMUM SPACING FOR MINIMUM INSERTION LOSS IN A TWO-DIODE SHUNT-ITERATED SWITCH

2.8 THREE-DIODE SHUNT-ITERATED SPST SWITCH

The three-diode shunt-iterated SPST switch is simply a higher isolation version of the two-diode iterated switch requiring more space and additional biasing and tuning circuitry. With 3 diodes spaced λ/4 apart, an isolation improvement as high as 50 dB can be realized over the two-diode switch at the same spacing. The design curves for a three-diode shunt-iterated switch are shown in Figures 2.8-1 and 2.8-3 and the equivalent circuit in both the pass and reject modes is shown in Figure 2.1-2f. As with the two-diode iteration, maximum isolation occurs at a spacing of λ/4.

Although at low frequencies (~10 MHz) other three-diode switch types can offer higher isolation, the three-diode shunt-iterated switch is theoretically frequency independent and rapidly outperforms other three-diode switches (such as a Pi or Tee) as frequency increases. Figure 2.8-1 illustrates the isolation of this switch as a function of both diode spacing and forward resistance. Like the two-diode shunt-iterated array, the three-diode shunt iteration has an insertion-loss response that is frequency sensitive and shifts drastically with increasing frequency and capacitance. However, unlike the two-diode switch, the three-diode version has a "double-tuned" insertion loss response that is no problem at lower frequencies but must be closely analyzed at high frequencies and capacitance values. The example

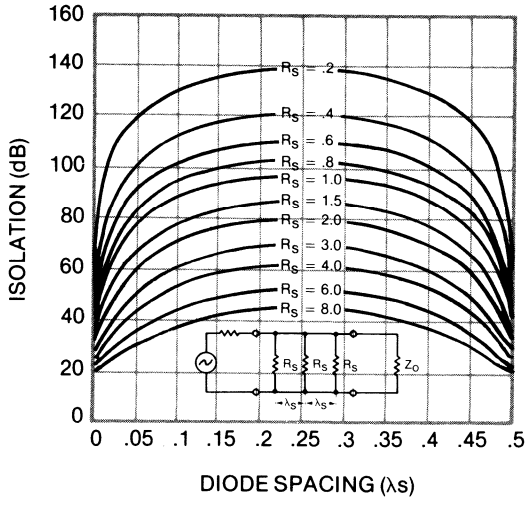


FIGURE 2.8-1 THREE SHUNT-ITERATED DIODES — ISOLATION VS SPACING

FIGURES 2.8-2 THREE SHUNT-ITERATED DIODES (C_j = 0.6 pF) — INSERTION LOSS VS SPACING

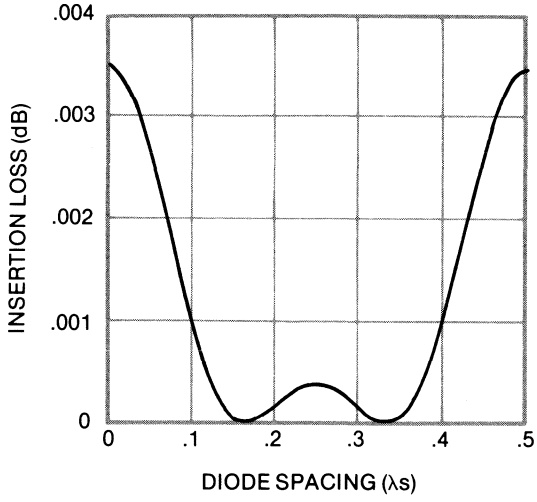


FIGURE 2.8-2a FREQUENCY = 0.1 GHz

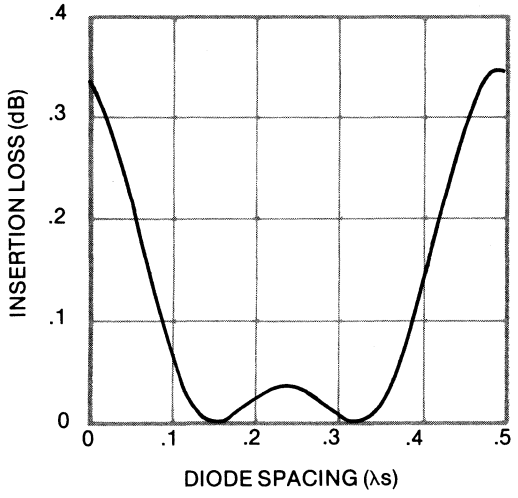


FIGURE 2.8-2b FREQUENCY = 1.0 GHz

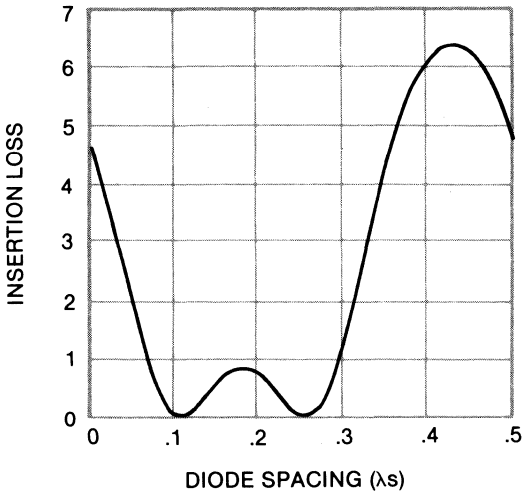


FIGURE 2.8-2c FREQUENCY = 5 GHz

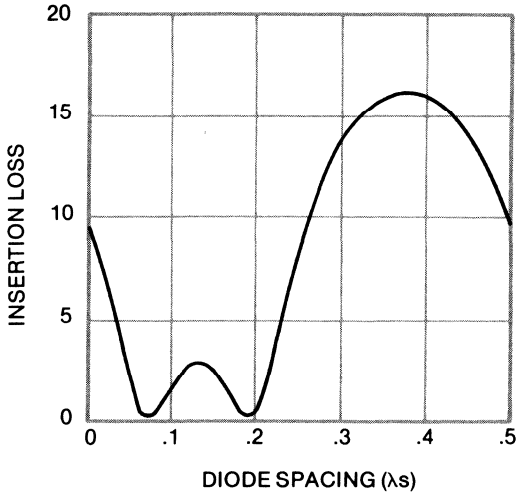


FIGURE 2.8-2d FREQUENCY = 10 GHz

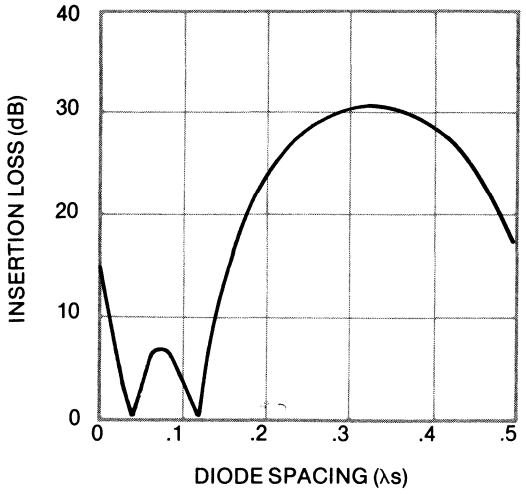


FIGURE 2.8-2e FREQUENCY = 20 GHz

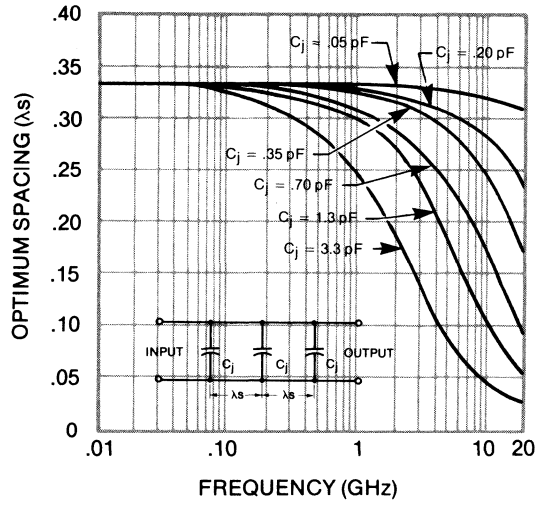


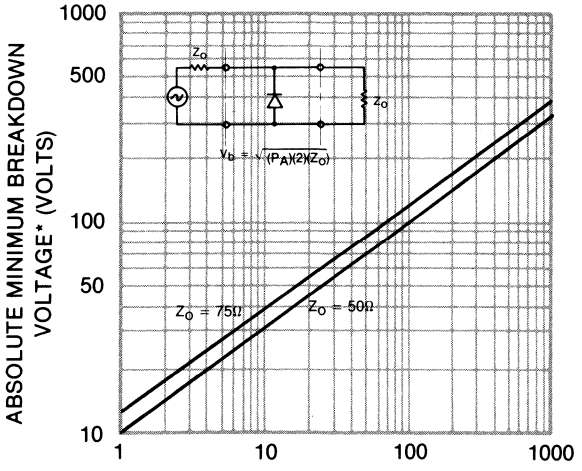
FIGURE 2.8-3 OPTIMUM SPACING FOR MINIMUM INSERTION LOSS IN A THREE-DIODE SHUNT-ITERATED SWITCH

shown in Figure 2.8-2 uses three diodes with C_j values of 0.6 pF, and plots insertion loss as a function of diode spacing. At 100 MHz, minimum values of insertion loss can be obtained with a diode spacing of either .165 λ or .335 λ. The values of insertion loss for any spacing, however, are insignificant at this frequency. At 10 GHz, minimum loss is achieved at a spacing of either .07 λ or .19λ. If the diodes were set at the classic λ/4 for maximum isolation, the insertion loss would be 8 dB. If this double-tuned response were ignored, and the diodes set perhaps .13 λ apart, almost 3 dB of loss would be incurred.

Figure 2.8-3 shows a plot of the optimum spacing for minimum insertion loss as a function of frequency and capacitance for a three-diode electrically-spaced shunt iteration. In this case, there are two spacing values for minimum insertion loss. This figure

represents only the wider spacing, because the wider spacing results in higher isolation in the reject mode. Like the two-diode iteration, the spacing for minimum loss theoretically results in a zero value for insertion loss.

The design procedure, then, for the three-diode shunt-iterated switch is similar to that of the two-diode version. Careful attention must be paid to the electrical spacing in order to minimize insertion loss.



*WHERE REVERSE BIAS VOLTAGE IS APPLIED THE "Y" AXIS MUST BE INCREASED BY THE VALUE OF APPLIED BIAS VOLTAGE

FIGURE 2.9-1 ABSOLUTE MINIMUM BREAKDOWN VOLTAGE* FOR A SHUNT MOUNTED DIODE AS A FUNCTION OF POWER AVAILABLE TO THE LOAD

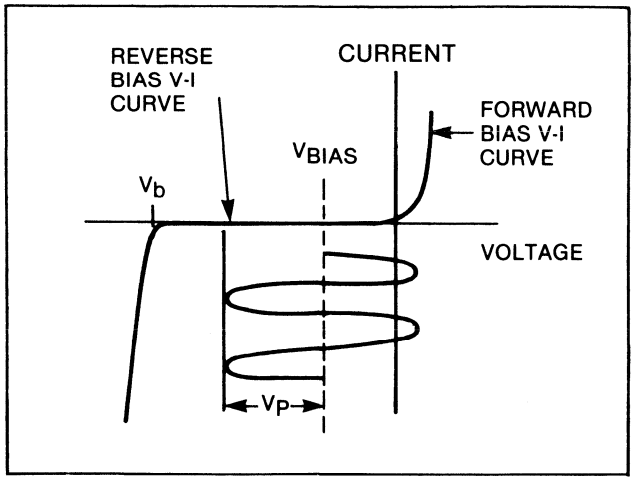


FIGURE 2.9-2 OPERATION AT HIGH RF VOLTAGE AND REVERSE BIAS

2.9 POWER DISTRIBUTION IN SHUNT DIODE SWITCHES

In the low-loss, or pass mode, power dissipation in a single, multiple or multiple-spaced (iterated) diode switch is rarely a concern. If the switch has a reasonably low insertion loss there is obviously very little energy either dissipated in the diodes or reflected back to the generator. However, there is concern that the power available from the source could be high enough to cause the switching diode or diodes to suffer catastrophic failure by being driven into reverse avalanche breakdown. The limiting factor here is the value of the device's breakdown voltage. Figure 2.9-1 shows the absolute minimum value of breakdown voltage required as a function of available peak incident power for a SPST shunt switch. It is assumed here that the switching time of the diode is much faster than a period of the incident frequency. Should the switching time be less than the RF period, the incident energy could forward-bias the diode. High insertion loss would occur and thermal considerations would then become necessary. In order to limit current flow and thus maintain low insertion loss, reverse-bias voltage is usually applied to the PIN. The amount of this bias must be added to the absolute minimum breakdown voltage. The condition for a high RF voltage drive with reverse bias is shown in Figure 2.9-2. It should be emphasized here that the minimum breakdown voltage given by the curve of Figure 2.9-1 is a value determined for device survival. The recommended breakdown voltage for high reliability must be a greater value than the sum of the DC reverse-bias

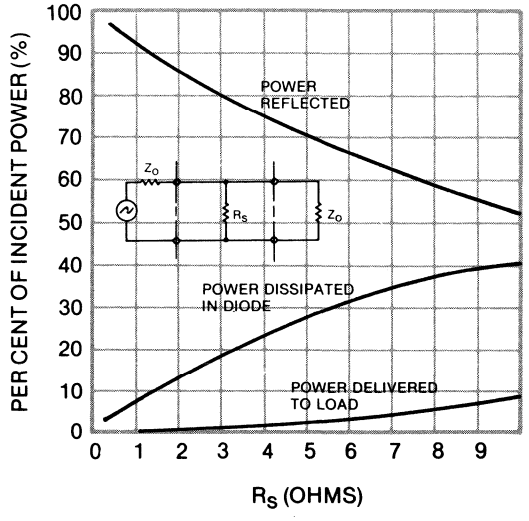


FIGURE 2.9-3 POWER DISTRIBUTION IN A SPST SINGLE DIODE SHUNT SWITCH AS A FUNCTION OF R_s

voltage (V_{bias}) and the peak to peak RF voltage ($2V_p$). To be practical, the maximum sustainable V_p for a given breakdown voltage, (V_b), and V_{bias}, must be determined empirically. Taking high-power loss data for the diode, including pulse length, RF frequency and its applicable duty cycle, is the most effective technique.

In the reject mode, care must be taken to prevent thermal destruction of the switching diode or diodes. The power distribution in a simple SPST single diode shunt switch is shown in Figure 2.9-3. The diode is represented here as a pure real resistance, typical of a forward-biased chip or packaged diode where all parasitics have been tuned out. It will be noted that the percent of incident power absorbed in the diode increases dramatically as the series resistance, R_S, of the device increases. Using this curve to determine the power dissipation in a particular device, one can decide if the diode selected is thermally adequate based on its rated thermal resistance and reference to Figure 2.9-4. This figure shows the maximum power that can be dissipated at various temperatures by a device with a particular thermal resistance, θ_{jc}.

In summary, the diode selected must not be driven into reverse avalanche breakdown by the available incident power when operating in the low-loss mode and must have a thermal resistance low enough to dissipate the required amount of power in the high isolation mode.

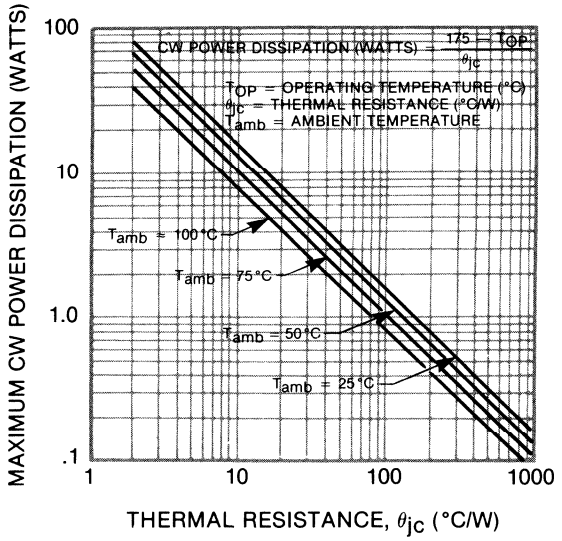


FIGURE 2.9-4 MAXIMUM CW POWER DISSIPATION FOR MA-4P SERIES OF PIN DIODES

Figure 2.9-5 shows the distribution of reflected and dissipated power in an iterated two diode shunt SPST switch. In this, the high-loss, or high isolation case, the diodes are spaced apart by λ/4, the spacing for maximum isolation, but not necessarily minimum insertion loss. For reasonable values of R_S, the isolation has been increased by a factor of 2, plus 6 dB over the isolation of a single diode shunt switch. This results in only .3% of the incident power being passed on to the load when two diodes

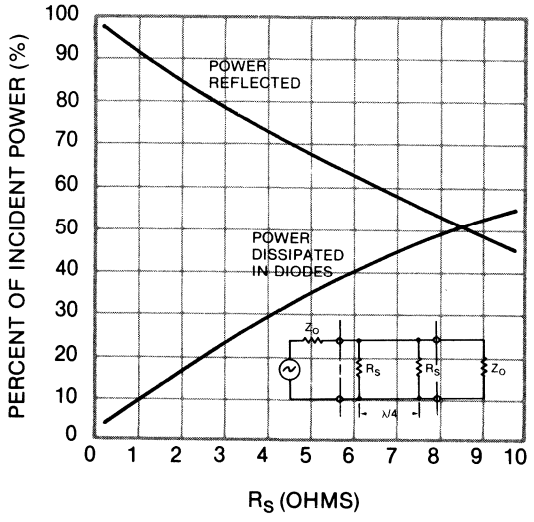


FIGURE 2.9-5 POWER DISTRIBUTION IN A SPST λ/4 SHUNT-ITERATED DIODE SWITCH AS A FUNCTION OF R_S

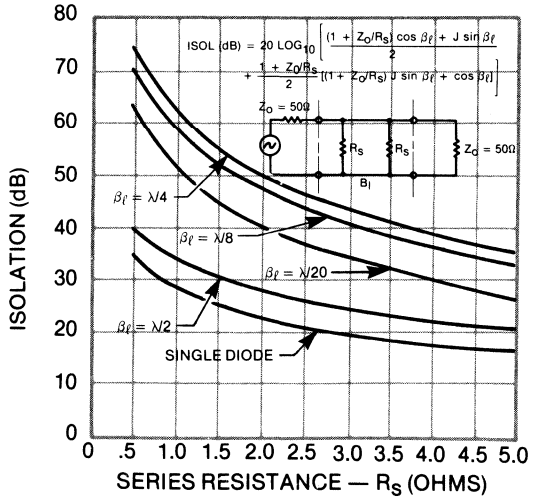


FIGURE 2.9-6 ISOLATION VS R_S* FOR A SINGLE DIODE SHUNT SWITCH AND TWO DIODE ITERATIONS

having R_S values as high as 10 ohms are used. The power dissipation in this particular two-diode array, has however, increased by over 30%. It is important to note that the dissipation distribution is far from equal between the two diodes. In fact, the diode closest to the generator absorbs as much as it would in a single-diode shunt switch. The remainder of the power is absorbed by the second diode. In the same two 10-ohm diode iteration, the first diode then absorbs 41% of the incident power and the second diode only 13%. This obviously leads to many trade-offs between R_S, isolation, thermal resistance, dissipation and, ultimately, cost. It becomes apparent that a more equal power distribution with reasonably high isolation could be accomplished using two devices of unequal R_S, with the diode of lower R_S closer to the generator.

Spacing is a factor in both the total dissipation and in the distribution of that dissipation. Maximum total dissipation occurs at the λ/4 spacing and the minimum total dissipation at zero, or λ/2 spacing. At λ/4 spacing, the first of two diodes of equal R_S absorbs far more power than the second. At a spacing of zero, the power is dissipated equally between the two.

The relative benefits in isolation between a simple shunt diode and a two-diode iteration at various spacings is shown in Figure 2.9-6. If physical circuit constraints will permit, two relatively inexpensive 6-ohm diodes can provide the same isolation as a single moderately priced device with an R_S of 0.5 ohm. Similarly, overall dc input power can be decreased and isolation be maintained, if two electrically-spaced diodes are driven with considerably less current than one with higher current.

A three-diode shunt iteration results in much the same power distribution as that of the two-diode iteration shown in Figure 2.9-5. Using three 10-ohm diodes spaced λ/4 apart, the power reaching the load is less than .01% of the incident power. The total array dissipation is just slightly greater than that of the two-diode array. For diodes with equal values of R_S, the diode closest to the generator dissipates by far the greater amount of the power. The second diode absorbs roughly the same percentage as in the two-diode array and the third diode absorbs only an extremely small amount of power.

2.10 POWER DISTRIBUTION IN SERIES DIODE SWITCHES

With series diode circuits, it is in the high-loss mode that peak available source power can drive series PIN switch diodes into reverse avalanche breakdown

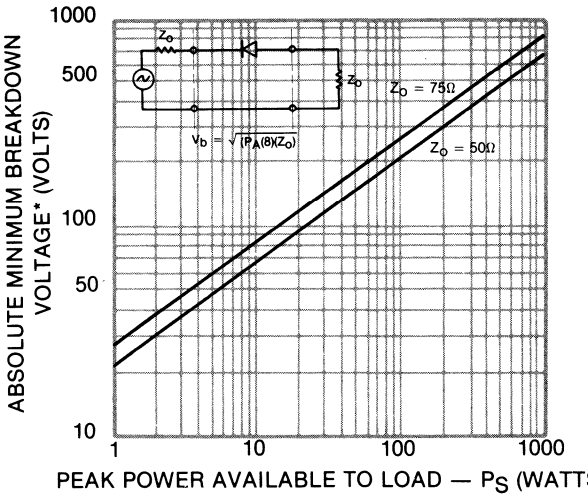


FIGURE 2.10-1 ABSOLUTE MIN. V_B* FOR A SERIES MOUNTED DIODE AS A FUNCTION OF PWR. AVAIL. TO THE LOAD

*Where bias reverse voltage is applied, the absolute minimum breakdown voltage must be increased by the amount of bias voltage.

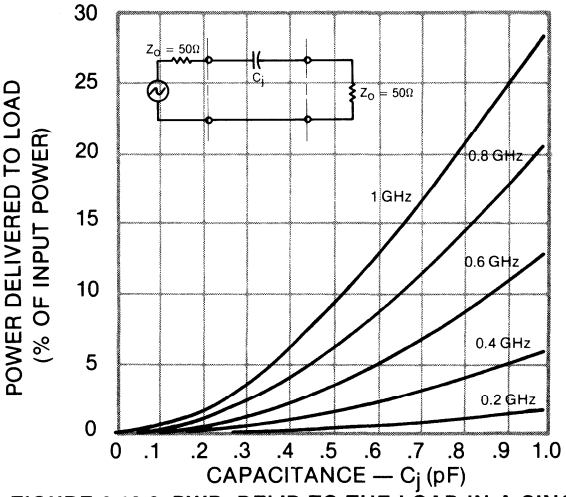


FIGURE 2.10-2 PWR. DEL'D TO THE LOAD IN A SINGLE-DIODE SERIES SWITCH AS A FUNCTION OF CAP. AND FREQ. — (REJ. MODE)

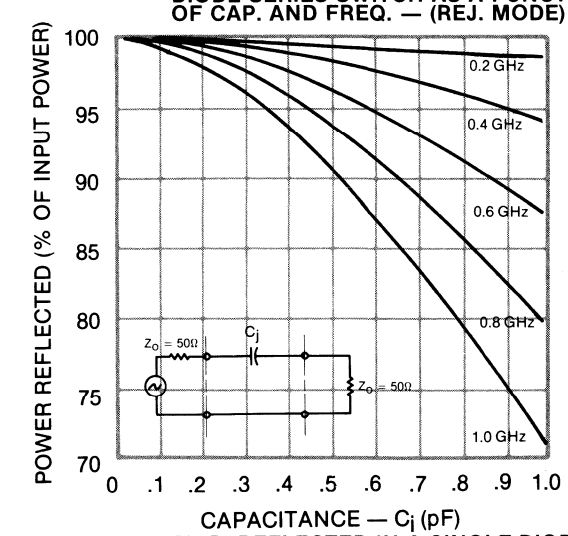


FIGURE 2.10-3 PWR. REFLECTED IN A SINGLE-DIODE SERIES SWITCH (REJ. MODE) AS A FUNCTION OF CAP. AND FREQ.

and subsequent catastrophic failure. Figure 2.10-1 shows the absolute minimum breakdown voltage necessary for device survival in a series diode switch. This voltage is twice that required for a single diode shunt circuit with the same peak power available from the source. The absolute minimum breakdown voltage for survival given by Figure 2.10-1 must be increased by the amount of any applied bias voltage. The actual recommended breakdown voltage for sustained operation must be an even greater value. To be practical, the maximum sustainable RF voltage for a given breakdown voltage and bias voltage must be determined empirically. As with shunt diode switches, taking high-power loss data for the diode, including pulse length, RF frequency and its applicable duty cycle is the most effective technique.

The power distribution for a single reverse-biased series chip or tuned packaged diode is frequency sensitive, but theoretically not dissipative, in nature. The curves of Figures 2.10-2 and 2.10-3 show this distribution. This corroborates the relationship shown by the design curves of Section 2.2 and evident here: high isolation as a function of changing frequency is not a strong point of the series switch.

In the pass mode, care must be taken to prevent thermal destruction of the series diode switch. The power distribution in a simple SPST single-diode forward-biased series switch is shown in Figure 2.10-4. The diode in this figure is assumed to be a pure resistance, typical of a forward-biased chip or packaged diode where all parasitics have been tuned out. It should be noted that the percentage of incident power absorbed in the diode increases significantly with increasing R_S, as it does with the parallel switch described in Section 2.9. Using the diode's rated thermal resistance when referring to Figure 2.9-4, one can then decide if the diode selected is thermally adequate.

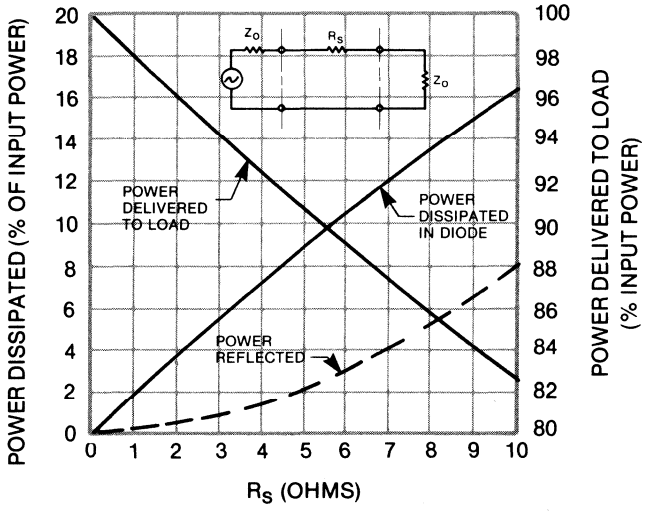


FIGURE 2.10-4 POWER DISTRIBUTION IN A SINGLE-DIODE SERIES SWITCH AS A FUNCTION OF R_S — PASS MODE

2.11 POWER DISTRIBUTION IN A PARALLEL-SERIES SWITCH

The power distribution of a parallel-series switch involves the principles of both Section 2.9 and 2.10. In the pass mode, where the shunt diode is located closest to the generator, the parallel device must have a sufficient breakdown voltage to prevent it from being driven into reverse avalanche. The curve of Figure 2.9-1 applies here. The amount of power incident on the second, or series diode can be determined by using the insertion loss curves of Figure 2.3-1a. Reference to Figure 2.10-4 will determine the amount of power dissipated in the series diode; reference to Figure 2.9-4 will determine if the device chosen is thermally adequate.

In the reject mode, the thermal acceptance of the initial shunt diode can be determined by using the curves of Figure 2.9-3 and 2.9-4. The power passed on to the series diode can be defined by using the isolation curves of Figure 2.3-1b. The minimum breakdown voltage for the series diode which will prevent avalanche drive can then be determined from Figure 2.10-1. The same type of single component analysis is appropriate for a series-parallel (series diode closest to the generator) switch.

2.12 DESIGN OF MULTITHROW SWITCHES USING PACKAGED DIODES WITH UNTUNED PARASITICS

This section will present some switch designs, highlight the various trade-offs and emphasize the effect of case parasitics on switch performance. The first design will be for a moderate bandwidth high-power, single-pole, three-throw (SP3T) switch centered at 1 GHz. It is stipulated that the transmission environment allows only shunt mounting and that the highest reasonable isolation is required, with loss kept at a minimum. The devices used will be mounted in case style 30 packages. (See Figure 6.2-2a for outline drawing.) The maximum power available from the generator is 500 watts.

From the preceding sections, it is apparent that multidevice iterations at specific electrical spacing offer significant advantages in isolation. Because of its relatively low R_S, high voltage breakdown and low thermal resistance, the MA-4P606-30* PIN was

*The suffix — 30 indicates case style 30.

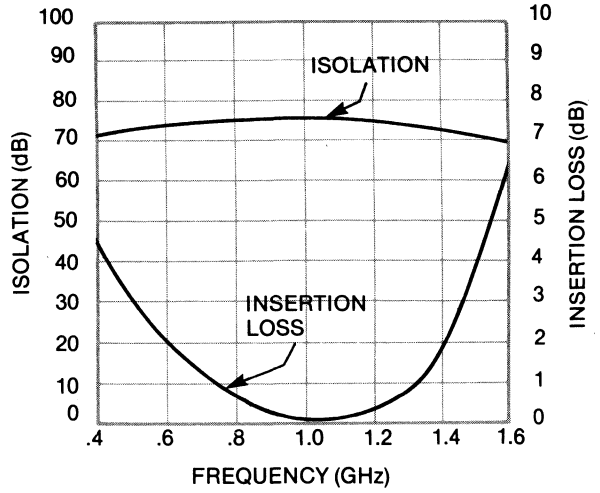


FIGURE 2.12-1 SP3T 1 GHz SWITCH — (2) MA-4P606-30 DIODES IN EACH ARM SPACED λ/4 APART — PARASITICS TUNED OUT

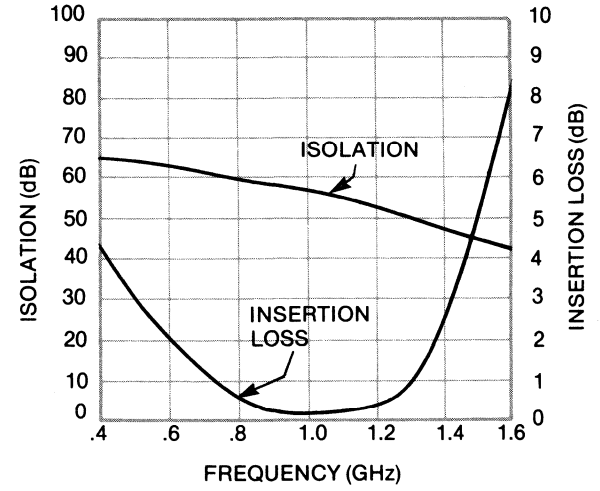


FIGURE 2.12-2 1 GHZ SP3T SWITCH — (2) MA-4P606-30 DIODES IN EACH ARM, SPACED λ/4 APART — PARASITICS UNTUNED

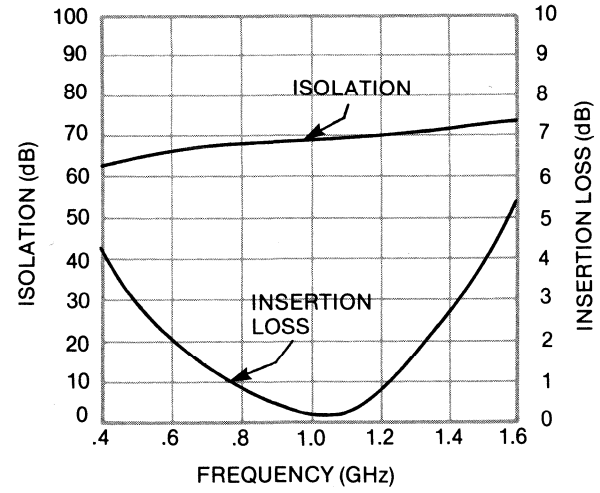


FIGURE 2.12-3 1 GHz SP3T SWITCH — (2) MA-4P606-30 DIODES IN EACH ARM SPACED λ/10 APART — PARASITICS TUNED OUT

chosen for the switch design. The initial SP3T design chosen incorporates 6 diodes (2 diodes in each path). The array in each path is spaced λ/4 from the switch junction in order to reflect a high impedance at that junction by the "OFF" switch arrays. If the two devices in each arm are spaced λ/4 apart, the maximum isolation will be obtained. Figure 2.12-1 shows the isolation and insertion loss performance that can be obtained if all diode parasitics are tuned out. (See Chapter 6 on Parasitic Tuning.) If the parasitics lead inductance (L_S) and package capacitance (C_P) are not tuned out at all, the performance shown in Figure 2.12-2 will prevail. Note here that the center frequency isolation has degraded by 18 dB, due primarily to the diode's L_S. This is because at 1 GHz, the inductive reactance in each diode is greater than three times as large as the device's series resistance. Even so, the switch performance is still acceptable. Reducing the spacing between diodes may become necessary when the physical size of the switch is a problem. (For example, at 1 GHz in a single medium TEM transmission line with air as the dielectric, a wavelength is 11.8 inches long.) Figure 2.12-3 shows the performance of the 6-diode SP3T switch with a spacing of only λ/10 between each diode set and with all parasitics tuned out. The performance of the same switch with all parasitics present is shown in the curves of Figure 2.12-4. Again, note the 16 dB performance degradation in isolation at center frequency, caused primarily by the diodes' lead inductance. However, if 1 dB of loss is acceptable, this still provides a good untuned 1 GHz switch with a minimum isolation of 48 dB and a bandwidth of 400 MHz. The final design configuration is shown in Figure 2.12-5.

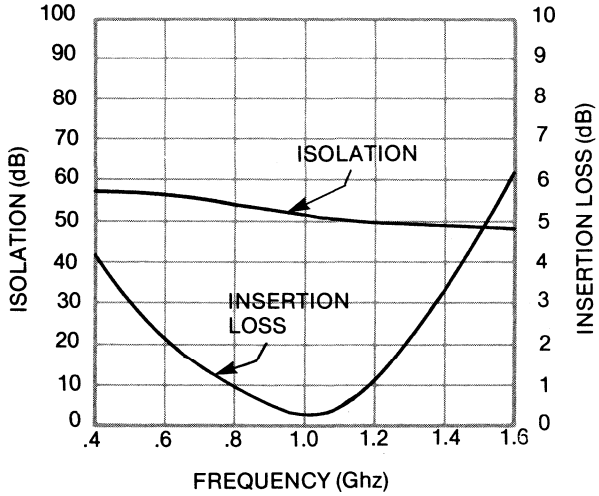


FIGURE 2.12-4 1 GHz SP3T SWITCH — (2) MA-4P606-30 DIODES IN EACH ARM SPACED λ/10 APART — PARASITICS UNTUNED

In a similar fashion, a higher isolation 9-diode (3 diodes per path) 1 GHz SP3T switch has been designed. Again MA-4P606-30 packaged diodes were used. Figure 2.12-6 shows the electrical performance of the switch with all parasitics tuned out and with λ/4 spacing between each diode in each array as well as between the diode sets and the juncture. For comparison, Figure 2.12-7 shows that the performance of the same switch without parasitic tuning has a 28 dB degradation in midband isolation.

If physical size becomes a problem, acceptable performance can be achieved if the spacing between the diodes in each array is reduced to λ/10. This is shown by the curves of Figure 2.12-8 for a SP3T switch with all parasitics tuned out. The same switch with untuned parasitics is shown in Figure 2.12-9. A 27 dB difference in isolation is realized with the tuned switch. However, if the 1 dB insertion loss is acceptable, this untuned 9 diode SP3T switch will provide a bandwidth of 400 MHz and a minimum isolation of 74 dB. The configuration is similar to that of Figure 2.12-5 except for an additional diode in each of the three arms.

In order to analyze a SPDT switch at 3 GHz, we will use as an illustration four MA-4P505-30 packaged PIN

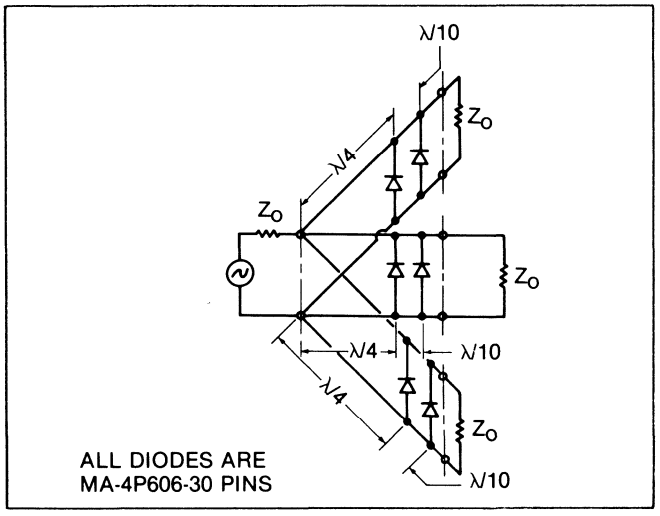


FIGURE 2.12-5 SP3T 6 DIODE 1 GHz SWITCH

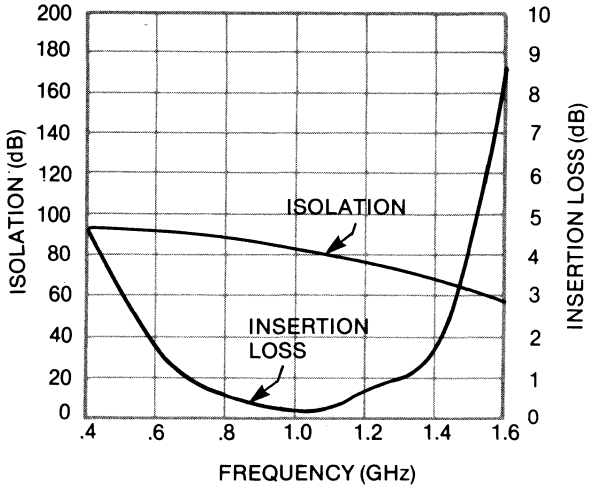


FIGURE 2.12-7 1 GHz SP3T SWITCH — (3) SHUNT DIODES IN EACH ARM SPACED λ/4 APART — PARASITICS UNTUNED

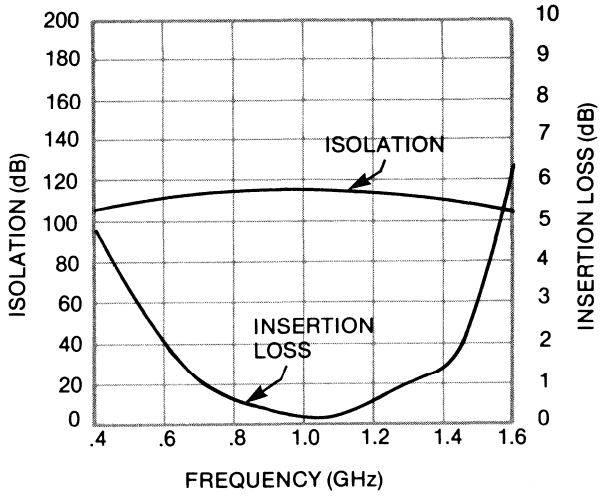


FIGURE 2.12-6 1 GHz SP3T SWITCH — (3) MA-4P606-30 DIODES IN EACH ARM SPACED λ/4 APART — PARASITICS TUNED OUT

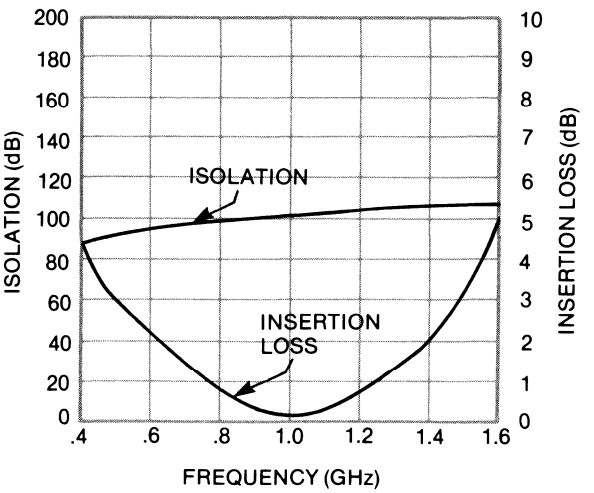


FIGURE 2-12-8 1 GHz SP3T SWITCH — (3) MA-4P606-30 DIODES IN EACH ARM SPACED λ/10 APART — PARASITICS TUNED OUT

diodes in a λ/4 spaced 2-diode iteration in each arm. Each diode array is spaced λ/4 from the switch juncture. With all parasitics of the case style 30 tuned out, the isolation and insertion-loss performance are as shown in Figure 2.12-10. As a result of tuning out just the lead inductance and leaving the case capacitance in the circuit, the switch performance would be as shown in Figure 2.12-11. Notice that there is no discernable degradation of the isolation, but the addition of C_p has significantly increased the insertion loss on the high end of the passband. Finally,

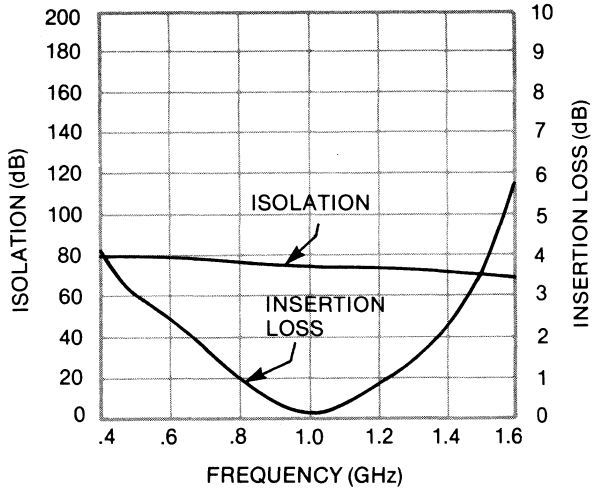


FIGURE 2.12-9 1 GHz SP3T SWITCH — (3) SHUNT DIODES IN EACH ARM SPACED λ/10 APART — PARASITICS UNTUNED

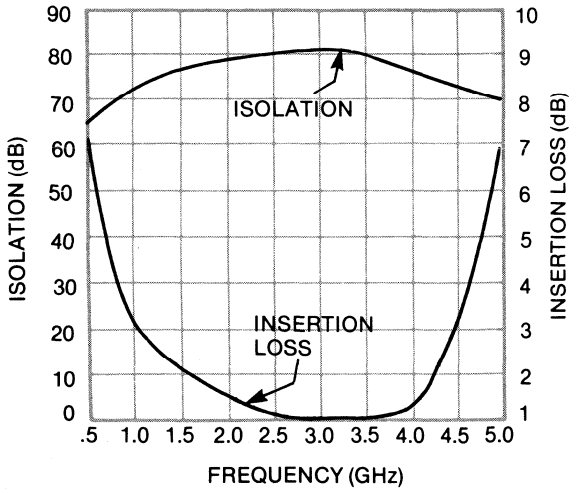


FIGURE 2.12-10 3 GHz SPDT SWITCH — (2) MA-4P505-30 DIODES IN EACH ARM SPACED λ/10 APART — PARASITICS TUNED OUT

Figure 2.12-12 shows the switch performance with both C_p and L_s untuned. Not only has the insertion loss at the upper end of the passband further degraded, but there has also been a disastrous drop in isolation with increasing frequency. This is because the inductive reactance for this case style at the upper band edge (5 GHz) is greater than 25 times as large as the PIN's series resistance. Thus, above several GHz the parasitics of a conventional untuned diode enclosure are almost intolerable.

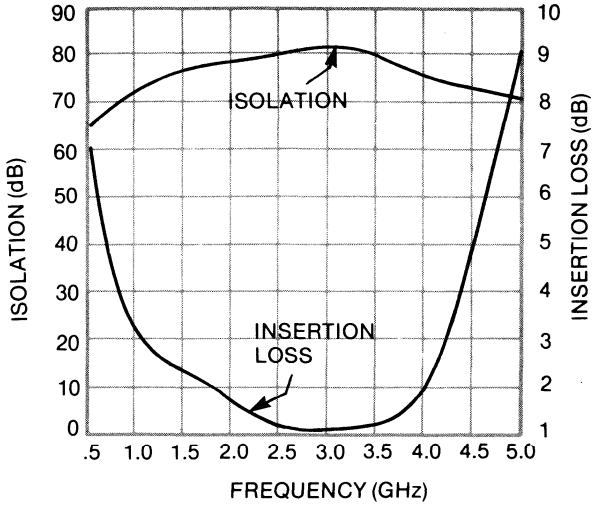


FIGURE 2.12-11 3 GHz SPDT SWITCH — (2) MA-4P505-30 DIODES IN ECH ARM SPACED λ/4 APART — L_s TUNED OUT

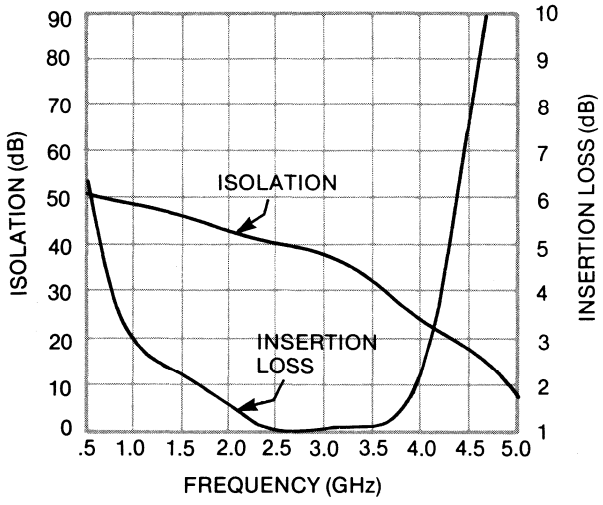


FIGURE 2.12-12 3 GHz SPDT SWITCH — (2) MA-4P505-30 DIODES IN EACH ARM SPACED λ/4 APART — PARASITICS UNTUNED

2.13 INTERMODULATION DISTORTION AND CARRIER LIFETIME

Intermodulation distortion can occur when multiple frequencies are incident on a PIN diode. This distortion takes the form of other frequencies which are sums and differences of both the input frequencies and/or their harmonics. In order to minimize this distortion, the carrier lifetime of the diode must be sufficiently long compared with a period of the lowest input frequency. Although hardware designs, power levels and design applications differ, a reasonable value for carrier lifetime as a function of input frequency would be five times the period of this frequency. A plot of this guideline is shown in Figure 2.13-1. For further reduction of the intermodulation distortion, a larger multiplier should be used for the determination of minimum carrier lifetime.

2.14 SWITCHING TIME AND BREAKDOWN VOLTAGE

The task of specifying switching time for a commercially available PIN diode can be confusing, since switching time is limited not only by device physics but also by the specific driver circuit used. However, the absolute lower limit of switching time, using the theoretical ideal driver which sweeps stored charge from the I-region instantaneously, is determined by the transit time, T_t, of the PIN diode. As explained in Chapter 1, transit time is defined as the time it takes for a carrier to transit the I-region at maximum saturated velocity, μ. Transit time is given by:

$$T_t\,(\text{sec}) = \frac{W_1}{\mu_s} \qquad (2\text{-}1)$$

where W_1 = the device I-region thickness (cm)

μ_s = maximum saturated velocity = 10^7 cm/sec

The I-region thickness, however, is directly related to the device breakdown voltage, V_b, by:

$$W_1\,(\text{microns}) \cong \frac{V_b}{20} \qquad (2\text{-}2)$$

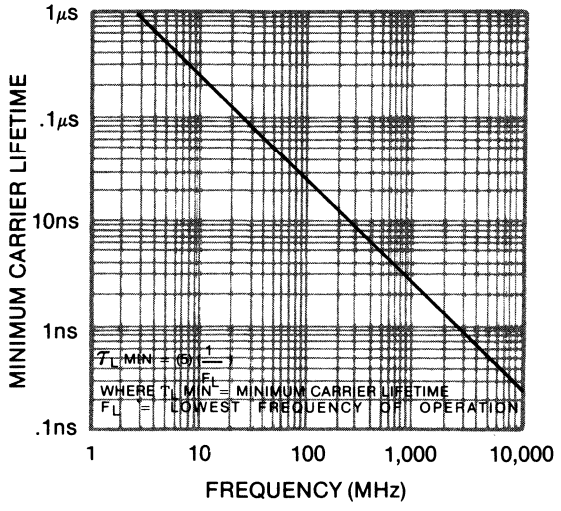


FIGURE 2.13-1 MINIMUM CARRIER LIFETIME AS A FUNCTION OF FREQUENCY

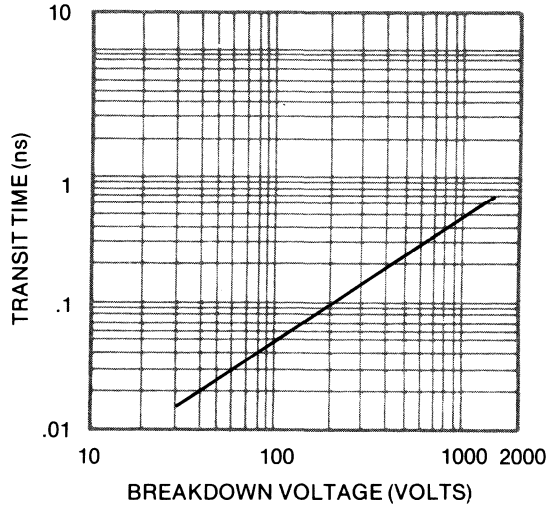


FIGURE 2.14-1 TRANSIT TIME AS A FUNCTION OF BREAKDOWN VOLTAGE

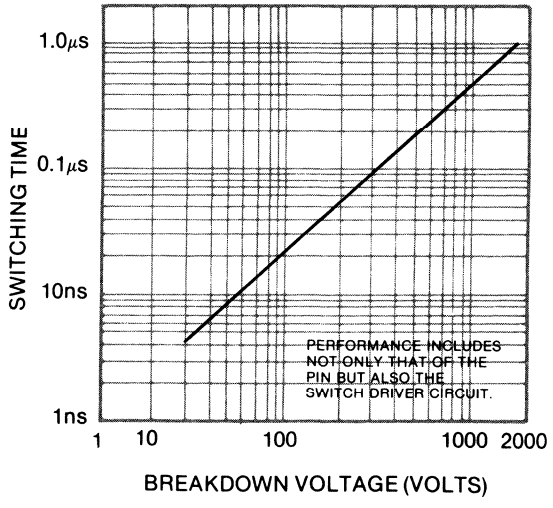


FIGURE 2.14-2 TYPICAL SWITCHING TIME AS A FUNCTION OF BREAKDOWN VOLTAGE*

By converting Equation 2-2 to cm and substituting into Equation 2-1 we have:

$$T_f(\text{ns}) = \frac{V_b}{2000} \qquad (2\text{-}3)$$

Figure 2.14-1 shows a plot of transit time as a function of breakdown voltage. In practice, a typical switching time that can be achieved with a reasonable driver circuit as shown in Figure 2.14-2, is as high as 1300 times the PIN diode's transit time. Nevertheless, as is shown in the figure, switching time is still proportional to the PIN's breakdown voltage.

2.15 SWITCHING DIODE SELECTION PROCEDURE

A recommended procedure for PIN diode selection is as follows:

(1) Configuration
Using the generalized design curves of Chapter 2 and the switch performance selection guide of Section 10-2, select the circuit configuration (e.g., series, parallel, series-parallel, iterated diode, etc.) that will best meet the insertion loss and isolation design goals.

(2) Breakdown Voltage
The minimum allowable breakdown voltage for the expected incident power must first be determined. Using the breakdown voltage curves of Figures 2.9-1 and 2.10-1 along with the applicable power distribution discussion (Section 2.9, 2.10 or 2.11), select the minimum value of breakdown voltage for the switching application. Again, it should be emphasized that the minimum breakdown voltage given by the design curves is a value that will only allow the device to survive. The **recommended** breakdown voltage for high reliability should be a greater value than that necessary for survival.

(3) Switching Speed
As described in Section 2.14, switching speed is a function of the PIN's breakdown voltage and of the characteristics of the switch driver. To determine typical switching speed for the V_b selected, refer to Figure 2.14-2. It should be kept in mind that while the switching speeds plotted in this figure are typical values, drivers can be designed that will result in faster switching performance. If the driver design is fixed and the switching speed is not adequate for the breakdown voltage chosen, a compromise must be reached. Return to step (1) and change the configuration.

(4) Capacitance Range
Using the capacitance selection curves of Figure 11.1-2,select the maximum total capacitance for the desired circuit bandwidth and maximum frequency.

(5) Isolation and Insertion Loss
Using the selection guide of Section 10.2, the specifications for standard PIN diodes as given in the matrix shown in Chapter 11, and the specific switch performance curves given throughout Chapter 10, choose the diode model and exact configuration for the application, taking into account the already selected V_b, T_s and C_t values. The design curves of Chapter 10 reflect use of either chips or packages with their parasitics tuned out (see Chapter 6). Where parasitic tuning is used, the maximum expected bandwidth is approximately 10% despite the magnitude of C_t as given by Figure 2 in the data sheet. Wider bandwidths will necessitate the use of chip diodes.

(6) Thermal Resistance
Refer to sections 2.9, 2.10 and 2.11 for the applicable power distribution curves that will enable you to determine the approximate amount of power that will be dissipated in each switching diode. The curves of Figure 2.9-4 will then be useful in checking on the maximum allowable thermal resistance for the application. The PIN diode chosen must have a thermal resistance that does not exceed this value or thermal destruction could result.

(7) Carrier Lifetime
The design guide for minimizing intermodulation distribution is given by the curve of Figure 2.13-1. The carrier lifetime of the device or devices chosen should be equal to, or greater than, the values given by the design curve.

(8) Final Design
If steps (1) thru (7) are completed to the satisfaction of the designer, the selection process is over. If not, a compromise in either configuration and/or specifications must be reached. As we have seen, the final choice of a PIN diode or diodes for a switching application depends on many factors. Parameter trade offs are a necessary part of device selection. In all probability, you will have to work through this selection procedure several times before selecting your PIN diodes and final design configuration.

PIN diode limiters

PIN diode limiters

3.1 LIMITER PROPERTIES

Often a component is needed to limit the amplitude of an RF or microwave signal to a level below a controlled threshold. Certain properties of PIN diodes are ideal for performing this limiting function. When a PIN diode is specifically designed to optimize its limiting properties it is usually called a limiter diode. The function of a limiter can best be illustrated by the plot of output power (P_{out}) vs input power (P_{in}) for an ideal limiter, as shown in Figure 3.1-1. Signals below a threshold power limit (P_{th}) pass through the limiter unattenuated. When P_{in} equals P_{th}, the output power saturates at a value which is not exceeded as the input power increases to higher levels. A practical limiter has some insertion loss at power levels below threshold and has a gradual transition into the flat leakage level portion of the P_{out} vs P_{in} curve. In addition, a practical limiter has a maximum level of isolation beyond which the output power will start to rise again in response to increased input power.

3.2 OPERATION

Most diode limiters are required to operate in a passive mode. That is, no external bias is applied to the diode before the RF power is incident on the limiter. For small RF signals, the limiter diode appears as a zero biased PIN diode in shunt with the RF transmission path. A good limiter diode must be in a minimum insertion-loss state at zero bias or have zero bias punchthrough for maximum performance. Special device processing is often needed to obtain the zero-bias punchthrough characteristic of limiter diodes.

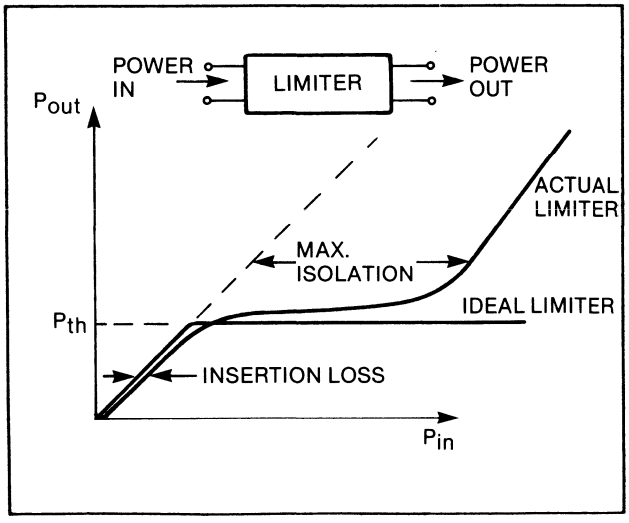


FIGURE 3.1-1 P_{out} VS P_{in} FOR AN IDEAL AND AN ACTUAL LIMITER

As the RF power increases, the diode will start to rectify. If a DC return is supplied to allow the rectification current to flow with minimum voltage drop, the diode will drive itself into forward bias as the input power increases. The threshold at which the device starts to limit is determined by the ease with which it will rectify the incoming RF signal. A typical 30 volt limiter diode in shunt with a 50 ohm line will start to limit at a power level well below 30 mW. Wider I-region, higher breakdown voltage limiter diodes will require higher power before they will limit. In order to achieve very low levels of flat leakage, a PIN and reverse polarity NIP can be used together to obtain rectification on both halves of the RF cycle.

The maximum isolation of a limiter diode is determined by its series resistance (R_S) at the maximum rectified current level. That is, the limiter appears as a forward biased PIN diode in shunt with the selected RF transmission structure. The lower the value of R_S, the higher the isolation value will be. A good limiter diode requires very little current to attain its minimum R_S state.

3.3 USAGE

Limiter diodes are most commonly used as protection devices for such sensitive receiver components as parametric amplifiers, mixers and detectors. Limiter diodes are increasingly used to protect small-signal bipolar transistors or GaAs FETs from the damage that can result from excessive input power.

A typical single diode limiter made from an MA-4L022-30 limiter diode and operatng at a frequency in X or Ku band will have the following specifications:

Insertion Loss	= 0.5 dB
Maximum Isolation	= 25 dB
Flat Leakage	= 30 mW maximum
Power Handling	= 1 watt CW or 100 watt pulsed for 1 μsec pulse duration

Similar specifications can be obtained at frequencies ranging from S band to Ku band. Limiters made with packaged diodes usually operate over a 10% bandwidth. By using diode chips in microstrip circuits, limiters can be made which exhibit similar performance over multioctave bandwidths.

PIN diode limiters

3.4 HIGH-POWER LIMITERS

In order to handle higher pulsed or CW input power levels, more than one diode can be used in a limiter design. The key to handling high power is to minimize power dissipation in the diode by reflecting most of the incident power. Designs should maximize the speed with which the limiter diodes turn on. When fully turned on in the high rectified current state, the limiter diode will reflect most of the incident power and absorb very little. As a result, the limiter diodes can withstand maximum input power when they are fully turned on. If a structure is not designed to encourage a rapid turn on, the limiter diodes can be damaged by the RF power before they are in the reflecting state. Some of the design schemes used for high power limiters are as follows:

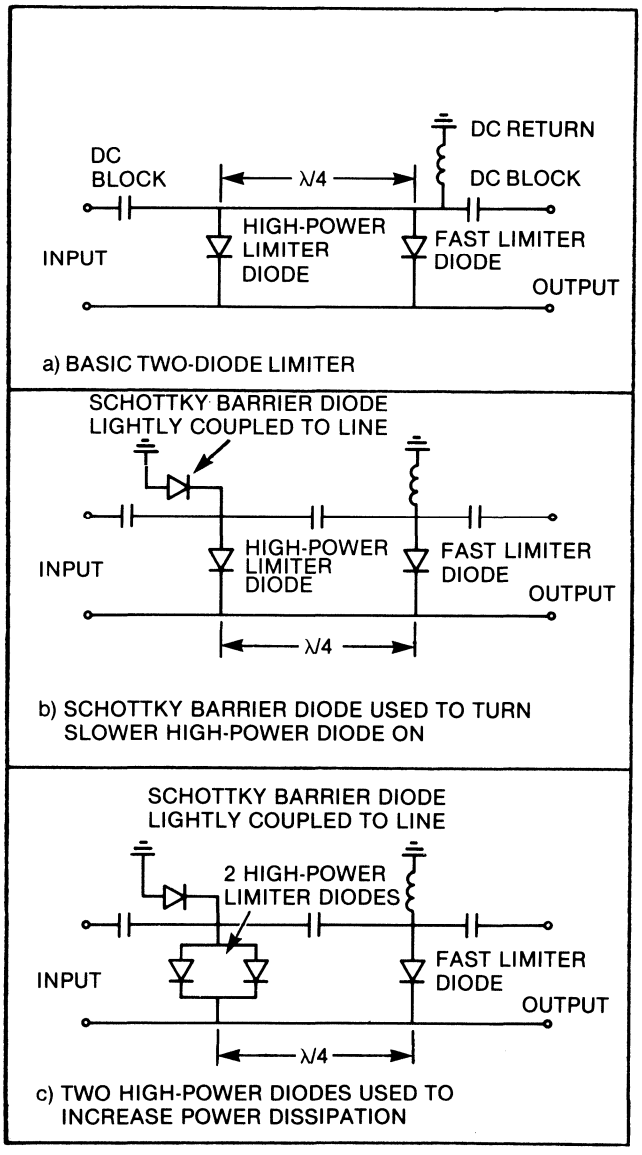


FIGURE 3.4-1 CIRCUIT CONFIGURATION FOR HIGH-POWER LIMITERS

(1) Larger junction area, higher power, slower turn on limiter diodes are located λ/4 in front of a high speed low power limiter diode. The faster diode helps to turn the slower diode on. Sometimes the bias path is directed to bias the slower diode with the rectified current of the faster diode. A limiter using this principle is illustrated in Figure 3.4-1a.

(2) Sometimes a Schottky barrier diode is lightly coupled to the RF line to provide additional rectification current for turning a slower diode on quickly. Such diodes can often generate up to 40 mA of DC bias current. Figure 3.4-1b shows this feature incorporated into a limiter design.

(3) Often higher power diodes are placed side by side in order to permit more power dissipation in the front diodes. The performance price of this scheme is usually increased insertion loss over a single diode design. A limiter utilizing this design technique is illustrated in Figure 3.4-1c.

These high power limiter design techniques can be used in waveguide, coaxial or microstrip designs. By using an MA-4L301-30 as the power diode and an MA-4L021-30 as the fast limiter diode, the following typical performance can be obtained at X-band frequencies.

Insertion Loss	= 0.5 dB
Maximum Isolation	= 40 dB
Flat Leakage Power	= 30 mW max
Power Handling	= 20 watts CW or 2 kW for 1 microsecond pulsewidths

The design principles for limiters are basically the same as for PIN diode switches. The insertion loss (low level) state is equivalent to having reverse biased PIN diodes in shunt with a transmission line. The only difference is that zero-bias, small-signal

parameters should be used for the limiter diode rather than the reverse-biased parameters commonly used in switches. The full isolation or maximum power handling state is equivalent to forward-biased PIN diodes in shunt with the transmission line. Instead of the driver bias current determining the R_S value, the rectification current value will determine the appropriate R_S to use. Otherwise, all isolation and power handling calculations are the same as for PIN diode switches. (See Section 2.9.)

The major differences between PIN diode switch design and PIN diode limiter design are in the rectification transients, which occur when input power over the limiting threshold is applied or removed from the diode. These transients are not easily calculated, and are even difficult to measure without disturbing the RF environment of the diode. As a result, it is common practice to calculate performance for both the low-level insertion loss and maximum isolation states and to observe the resulting transient performance. The two transients involved are the turn-on transient and the turn-off, or recovery, transient. In the turn-on transient, the diode changes from a zero-bias state to a full rectified-current state. During this transient, the diode passes through its full range of isolation. The transmitted power, reflected power, and power dissipated in the diode will vary during the transient. As a result, a portion of the RF energy leaks through in a pulse at the leading edge of the waveform. This pulse, illustrated in Figure 3.5-1, is known as the spike leakage of the limiter and is usually specified either in ergs or by amplitude and duration specifications. The spike leakage is generally much smaller than the spike leakage which occurs with gas TR tubes used as receiver protectors.

The second transient, or recovery transient, of the limiter occurs when the high power RF is turned off and the diode must change from a forward bias state to a zero-bias state. This transient is governed by the recombination of carriers in the intrinsic region and generally follows an exponential curve. Its time constant is influenced by both the minority carrier lifetime of the diode and the time constant of the DC bias circuit. In power testing limiters, the recovery transient shown in Figure 3.5-1c is usually monitored. The recovery transient of a limiter will usually degrade at power levels slightly below power levels where irreversible damage will be done to the diode. As a result, the recovery transient can be used to test limiters for maximum power handling without destroying them.

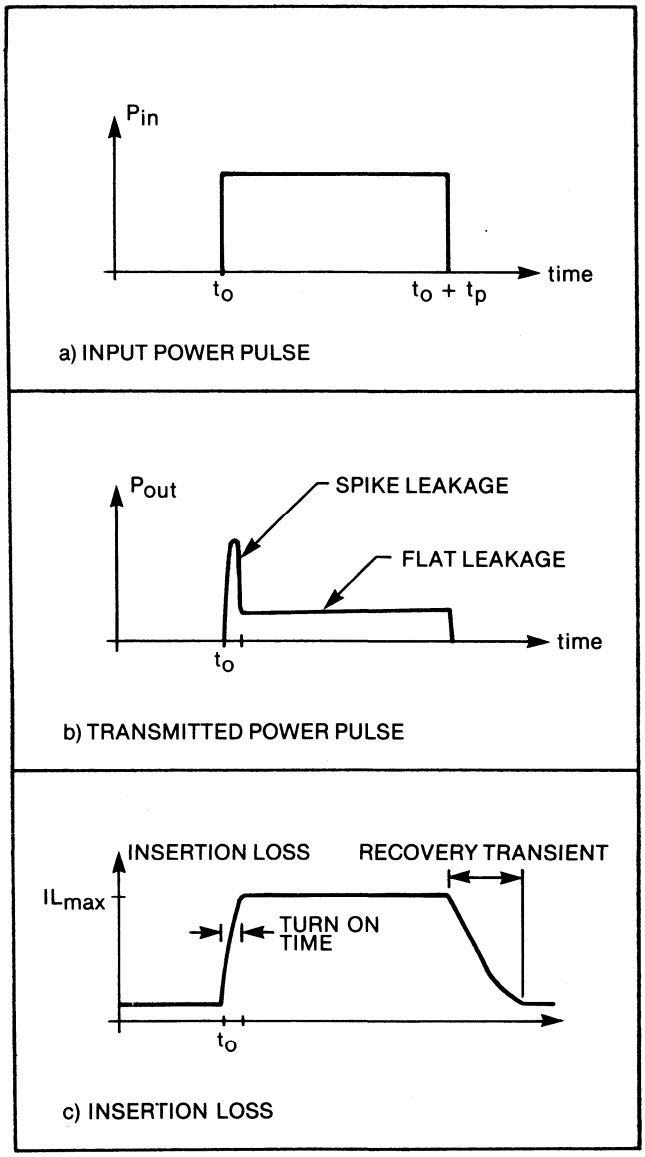


FIGURE 3.5-1 INPUT POWER, TRANSMITTED POWER AND INSERTION LOSS VS TIME FOR A TYPICAL PULSED LIMITER

PIN diode limiters

3.6 LIMITER DIODES

Microwave Associates produces a special group of PIN diodes for limiter applications. Each of these diodes is designed for minimum insertion loss at zero bias, rapid turn on and maximum isolation. The diodes are available in both case style 30 ceramic packages and as chips for hybrid circuits. Other case styles are available on request. Table 3-A provides detailed specifications and typical performance for these limiter diodes.

TABLE 3-A. LIMITER DIODES

Packaged Diode[1] Model Number	Chip Diode[1] Model Number	Min.[2] Breakdown Voltage (Volts)	Max.[3] Total Zero Voltage Capacitance (pF)	Max.[4] Series Resistance (Ohms)	Max.[5] Thermal Resistance (°C/W)	Typical Pulsed Power[6] (Watts)
MA-4L011-30	MA-4L011-134	20	.40	2.0	70	80
MA-4L021-30	MA-4L021-134	30	.40	1.5	60	100
MA-4L022-30	MA-4L022-134	30	.30	2.0	60	100
MA-4L031-30	MA-4L031-134	40	.40	1.5	40	200
MA-4L032-30	MA-4L032-134	40	.30	2.0	40	200
MA-4L101-30	MA-4L101-134	100	.30	1.7	30	1000
MA-4L301-30	MA-4L301-134	200	.35	1.7	25	2000

NOTES:

1. Packaged diodes are in case style 30. Other case styles are available on request. Diode chips are in the style 134 configuration.
2. I_r = 10μA
3. For chip diodes, subtract 0.18 pF
4. I_f = 10 mA, F = 500 MHz
5. In the case of chips, each chip must be bonded to an appropriate copper heat sink.
6. Pulse length of 1μsec and duty cycle less than 1%.

matched attenuators

4.1 DISCUSSION

This chapter describes another application of the PIN diode; a current variable attenuator which is matched throughout its attenuation range. We will examine a typical requirement for an IF attenuator from initial design through final performance results. To highlight design limitations, two general avenues of approach will be analyzed; the bridged TEE attenuator and the PI attenuator.

4.2 DESIGN CONSIDERATIONS

The following electrical specifications apply:

Frequency	70 MHz ±20 MHz
Flatness	±0.1 dB
Input Power	0 dBm typical
Return Loss	≥18 dB minimum (Input and Output)
Attenuation Range	1.5 dB to 20 dB
2 Tone Intermodulation	≥—60 dB below carrier (dBc)

The prime factors that will be considered are:

1) Ease of manufacture — No highly specialized labor or expensive components can be tolerated.

2) High rate of repeatability — Since this attenuator will be used in a cascaded IF system, each attenuator must react alike (within close tolerances) or dynamic range will be impaired.

3) Single lead for bias and/or controls.

Both bridged TEE and PI attenuators will be designed using Microwave Associates PIN diodes.

4.3 BRIDGED TEE ATTENUATOR

The schematic of Figure 4.3-1 shows a bridged TEE attenuator circuit. In this configuration, the resistor values of the two series resistors (R_0) are always set equal to the source and load impedance (Z_0). The bridged TEE attenuator requires the other resistor values (R_1 and R_2) to vary according to the following relations:

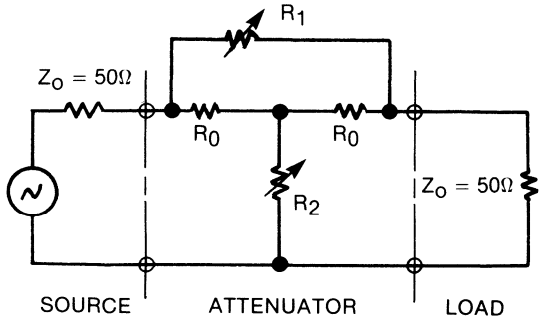


FIGURE 4.3-1 BRIDGED TEE ATTENUATOR

$$R_1 = Z_0\left(10^{\frac{dB}{20}} - 1\right) \quad (4\text{-}1)$$

$$R_2 = \frac{Z_0}{\left(10^{\frac{dB}{20}} - 1\right)} \quad (4\text{-}2)$$

The calculated resistance values for a matched 50 ohm bridged TEE attenuator are shown in Table 4-A.

TABLE 4-A COMPONENT VALUES FOR MATCHED 50 OHM BRIDGED TEE ATTENUATOR

Attenuation (dB)	R_1 (Ohms)	R_2 (Ohms)
1	6.1	409
2	13	193
3	21	121
4	29	86
5	39	64
6	50	50
8	76	33
10	108	23
12	149	16.8
14	201	12.5
16	266	9.4
18	347	7.2
20	450	5.5

The Microwave Associates' MA-47123 low cost general purpose PIN control diode which is housed in the axial lead case style 139, is well suited for use in a bridged TEE attenuator. (The MA-47123 is one of ten standard diode types manufactured by the Microwave Associates HVDO-High Volume Device Operation.) As a resistive element, impedance changes of 800:1 may be realized throughout the current range of 1μA to 50 mA. If in Figure 4.3-1, two MA-47123 PIN diodes, D_1 and D_2, are substituted for the resistor values, R_1 and R_2 respectively, and the results are plotted on log-log paper, a nearly straight line relationship appears up to about 3 mA, as shown in Figure 4.3-2. It should be noted, however, that above 3 mA the attenuator's characteristic curve departs from the straight line relationship. This is due to the log R_s vs I_f characteristic curve of the MA-47123 in conjunction with both the bridged TEE configuration and the chosen values of characteristic impedance, Z_0 and R_0. Figure 4.3-3 shows the typical

log R_S vs log I_f characteristic curve of the MA-47123 PIN diode measured at a frequency of 100 MHz. In order to determine this curve, 50 devices were measured at various forward currents. The total variation between all devices at specific currents is also illustrated by Figure 4.3-3.

The departure from a straight line at 3 mA does occur past the 20 dB attenuation design criteria.

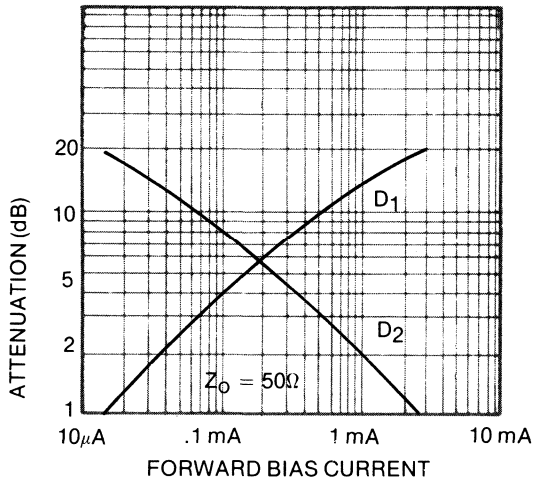


FIGURE 4.3-2 ATTENUATION VS DIODE CURRENTS FOR A MATCHED BRIDGED TEE ATTENUATOR USING MA-47123 PIN DIODES

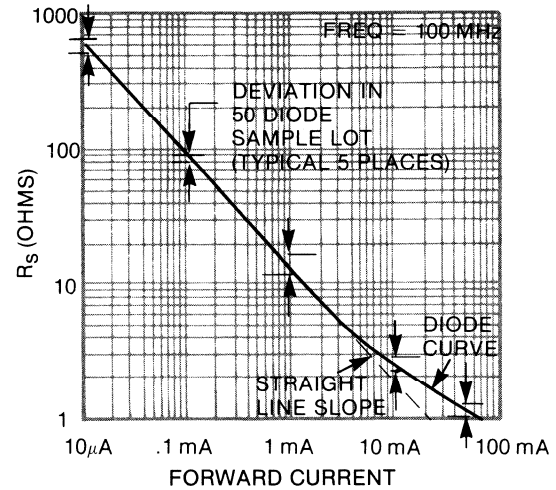


FIGURE 4.3-3 TYPICAL R_S VS I_f FOR AN MA-47123 PIN DIODE

However, at the higher levels of attenuation, the series diode is forward biased so slightly in its 50 ohm environment, that it is actually being influenced by the pumping action of the 0 dBm input signal. This results in a return loss at high attenuation levels that is less than the desired 18 dB. Additionally, measurements of two tone intermodulation revealed that our —60 dBc design goal was not realized across the full attenuation range. (At zero dB attenuation, the two tone intermodulation was lower than —60 dBc but as attenuation increases, it gradually degrades to a value of approximately —45 dBc at the 20 dB attenuation level).

Although there is excellent diode repeatability between different MA-47123 diodes, the design will not meet the criteria established in Section 4.2 for three reasons. First, at high attenuation levels the return loss is too low. Second, the two tone intermodulation level is too high. Third, the biasing constraints present a drive problem. While the forward bias current of D_1 goes from 10μA to 3 mA (300:1 change), the current of D_2 must change by the complementary range of 3 mA to 10μ (also a 300:1 change). Any driver circuit that would accomplish this would violate the design restriction of **a single bias lead.**

If multiple bias leads were acceptable but return loss or intermodulation performance could not be compromised, some changes could be attempted. One obvious change is the value of Z_O (and, as a result, R_O). In an attempt to improve performance, the bridged TEE attenuator was redesigned using a value of $Z_O = R_O = 150$ ohms, instead of 50 ohms, and an appropriate set of PIN diodes (MA-47083). A model was built and measured. The return loss and flatness response as a function of attenuation are shown in Table 4-B. The data in the table is taken over the frequency range of 50 to 90 MHz.

TABLE 4-B 150 OHMS BRIDGED TEE ELECTRICAL PERFORMANCE

Attenuation (dB)	Return Loss (dB)	Flatness (dB)
2	20	—.02
4	24	—.03
6	24	—.05
10	26	+.10
15	24	+.25
20	24	+.32

It will be noted that the flatness is within our design goals up to an attenuation level of 10 dB. Above this level the attenuation flatness decays badly. The reason for this is the direct result of the relative magnitude of the junction reactance of D_1 and the reactance of both diodes' case capacitance in conjunction with the chosen Z_O (150 ohms). This points out one of the pitfalls in matched PIN attenuator design. As Z_O is allowed to increase, the capacitive reactances associated with the diodes deteriorate the flatness of the attenuator.

4.4 PI ATTENUATOR

The schematic of Figure 4.4-1 (right) shows a PI attenuator circuit.

The unbalanced PI attenuator requires resistor values that vary in accordance with the following equations:

$$R_p = Z_O \left[1 + \frac{2}{\left(10^{\frac{dB}{20}} - 1 \right)} \right] \quad (4\text{-}3)$$

$$R_S = \left(\frac{Z_O}{2} \right) \left[\frac{\left(10^{\frac{dB}{10}} \right)^2 - 1}{\left(10^{\frac{dB}{10}} \right)} \right] \quad (4\text{-}4)$$

The calculated resistance values (R_p, R_S) for the matched 50 ohm PI attenuator are shown in Table 4-C.

TABLE 4-C COMPONENT VALUES FOR MATCHED 50 OHM PI ATTENUATOR

Attenuation (dB)	R_p (Ohms)	R_S (Ohms)
1	870	5.7
2	436	11.6
3	292	17.8
4	221	24
5	178	30
6	150	38
8	116	53
10	96	71.2
12	83	93
14	75	120
16	69	154
18	64	196
20	61	248

From the R_S vs I_f curve for the MA-47123 PIN diode, (Figure 4.3-3) we saw that at forward bias diode currents of about 3 mA and above, R_S becomes non-linear and deviates from the desired straight line relationship. For the PI attenuator, a diode choice will be made that will allow a linear relationship at I_f currents in excess of 30 mA. One such device is the MA-47111. This diode has an especially long minority carrier lifetime which is well suited for low frequency operation. (As discussed in Section 2.13, if a diode's minority carrier lifetime is significantly larger than one period of the applied RF, intermodulation distortion will be minimized.) Figure 4.4-2 shows the typical log R_S vs log I_f characteristic curve of the MA-47111 PIN diode measured at a frequency of 100 MHz. Fifty devices were measured at various forward currents to yield this typical curve. Also shown in Figure 4.4-2 is the total variation between all measured devices at specific forward currents.

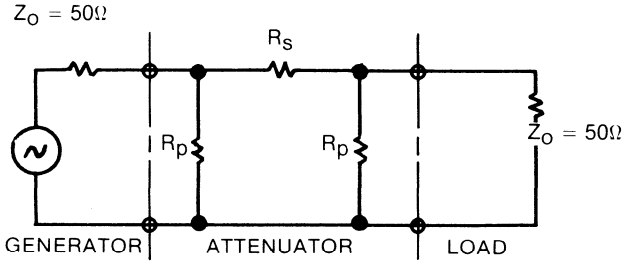


FIGURE 4.4-1 PI ATTENUATOR

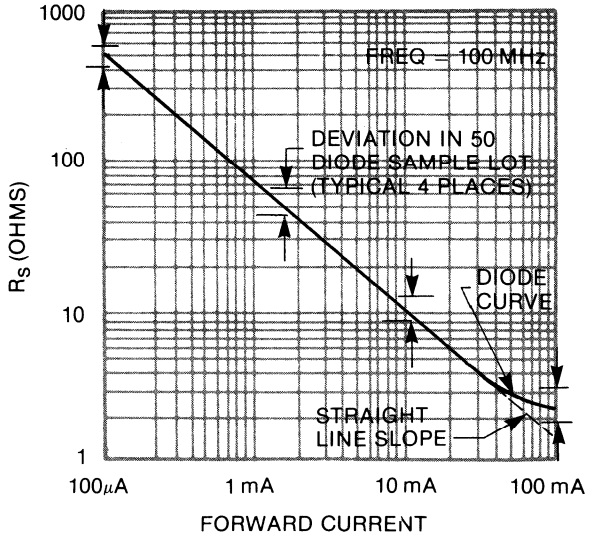


FIGURE 4.4-2 TYPICAL R_S VS I_f FOR AN MA-47111 PIN DIODE

The diode curve indicates a deviation from a straight line at approximately 40 mA. Even at a forward current of 70 mA ($R_S \cong 3\Omega$), the amount of departure from the straight line is only about 27%, which is considerably lower than the many other diode types that were plotted in this fashion.

Three MA-47111 PIN diodes were used to replace the resistors shown in the PI attenuator of Figure 4.4-1. The complete RF circuit including diodes, chokes and blocking capacitors is shown below in Figure 4.4-3.

The value of current necessary for both the series and parallel diodes as a function of attenuation was determined from the measured diode performance curves and is shown at right in Figure 4.4-4. The extremes in diode resistance at low attenuation levels (5.7 ohms to 877 ohms at a 1 dB level) require currents of approximately 50μA in the parallel diodes and 26 mA in the series diode. Using the above configuration, initial electrical measurements were taken over the 50 MHz to 90 MHz frequency range and recorded in Table 4-D.

As may be seen from this table, the control voltage is extremely non-linear as a function of attenuation. To prevent this, a carefully controlled driver circuit can be used. Not only will the non-linearity be greatly reduced with an appropriate driver, but also the gain variation will be reduced when this attenuator is used in an AGC controlled IF amplifier. The final driver design chosen was the anti-log driver shown in Figure 4.4-5. This was used in conjunction with the attenuator configuration of Figure 4.4-3.

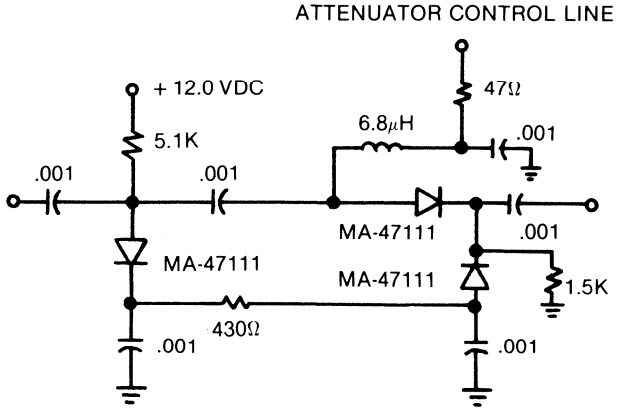


FIGURE 4.4-3 MATCHED ATTENUATOR — PI CONFIGURATION

TABLE 4-D MATCHED PI ATTENUATOR — INITIAL ELECTRICAL PERFORMANCE

Attenuation (dB)	Attenuator Control Voltage (Volts)	Return Loss (dB)	Flatness (dB)
1.3	20.00	14	.05
2	11.66	15	.01
3	10.54	20	.05
6	7.39	24	.05
9	5.33	22	0
12	4.53	24	0
15	3.69	30	0
18	3.37	30	.02
20	3.24	28	.03

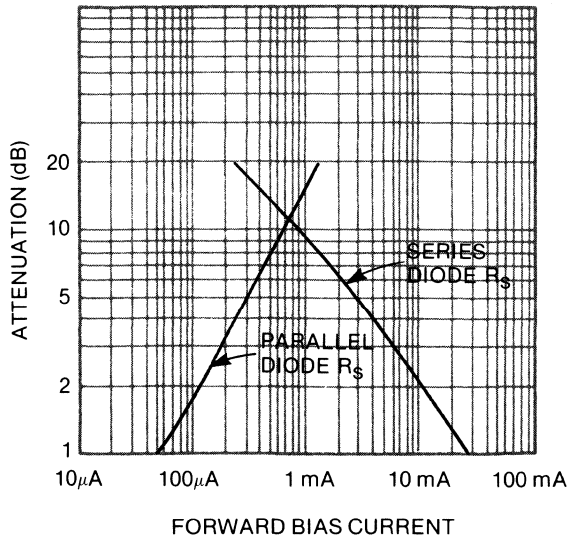


FIGURE 4.4-4 ATTENUATION VS DIODE CURRENTS FOR A MATCHED PI ATTENUATOR USING MA-47111 PIN DIODES

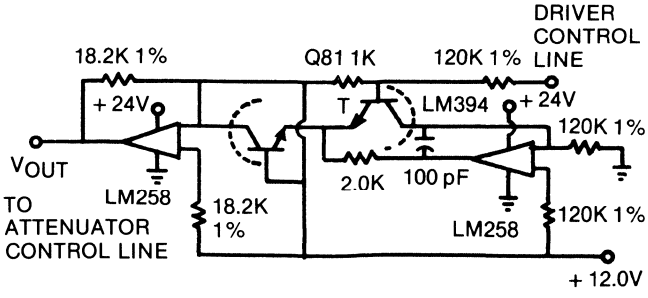


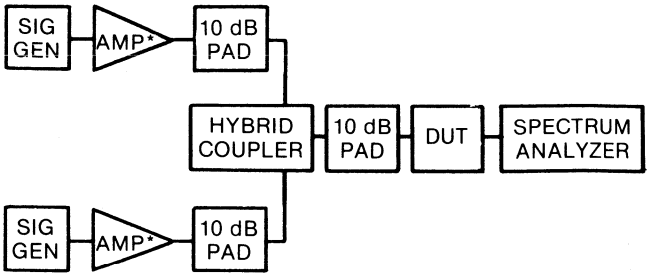
FIGURE 4.4-5 ANTILOG DRIVER CIRCUIT

Except for low return loss at small attenuation values, the results of Table 4-D are indeed quite encouraging. Note also that unlike the bridged TEE design, it is practical to achieve the necessary control of attenuation using one control line and one bias line. The departure from predicted return loss performance necessitated a close examination of the components used in the model. Table 4-C shows that at the lowest attenuation value, the diode (and all series components) must exhibit a series resistance of only 5.7Ω. Upon examination it was discovered that the disc capacitors used in the initial PI attenuator model represented a significant portion of this resistance.

Careful reconstruction of the attenuator using stripline techniques, which employ chip capacitors and metal-film resistors, resulted in improved return loss results without any degradation to transmission loss performance. This final transmission and reflection performance is shown in Table 4-E.

Two-tone intermodulation tests were performed on this attenuator using the test set up shown and the definitions given in Figure 4.4-6. Table 4-F shows the test results. The intermodulation levels of this table are referenced to the level of the signal generators shown in the test set and defined as dB below the incident carrier (dBc).

The completed PI attenuator was tested from 10 MHz to 100 MHz. Slight alterations in the low-pass filtering structure used in the control line allowed the matched PI attenuator to perform within the original design criteria over this entire 90 MHz band.



2ND ORDER = F_1 (35 MHz) + F_2 (34 MHz) = 69 MHz
3RD ORDER = F_1 (70 MHz) ± $2F_2$ (71 MHz) = 69 OR 72 MHz

*Mini-Circuits Lab. ZHL Amplifier (16 dB Gain)

FIGURE 4.4-6 INTERMODULATION DISTORTION TEST SET

TABLE 4-E MATCHED PI ATTENUATOR FINAL TRANSMISSION AND REFLECTION PERFORMANCE

Attenuation (dB)	Return Loss (dB)	Flatness (dB)
1.3	21	.05
2	23	.01
4	26	.04
6	21	0
10	24	0
14	30	0
20	22	0.3

TABLE 4-F MATCHED PI ATTENUATOR — TWO TONE INTERMODULATION LEVELS

Attenuation (dB)	2nd Order Intermodulation (dBc)	3rd Order Intermodulation (dBc)
1.2	≥ —70	NONE VISIBLE
10	—65	NONE VISIBLE
20	—60	—65
30	—58	—65

PIN measurements

5.1 DISCUSSION

This chapter will describe the classic and most important PIN measurement techniques. Relatively simple measurements such as breakdown voltage, leakage current, and capacitance have been purposely omitted.

5.2 SERIES RESISTANCE (R_S)

The classic method of determining the series resistance of a PIN diode is to resonate the device under test in a coaxial structure and measure the voltage transmission loss ratio. Historically, the measurement has been made at 500 MHz, but useful measurements can be made up to about 2000 MHz. All that is needed is an understanding of the diode's equivalent circuit and a practical definition of the measurement. A typical heterodyne coaxial R_S test set is shown below in Figure 5.2-1.

The signal oscillator is set to the desired test frequency, and its power level adjusted so that approximately 0 dBm is incident on the diode under test (DUT). The beat oscillator is set 30 MHz from the test frequency and the 30 MHz IF amplifier is used as the test set indicator. The R_S measurement is performed on a forward biased PIN or NIP. The DUT is shown in equivalent circuit form in Figure 5.2-2. It should be pointed out here that the equivalent circuit for a device biased only slightly in the forward direction (drawing less than 100 microamperes) to reverse breakdown, differs and thus changes the method by which R_S is determined.

Simple calculations show that at 500 MHz, using any common microwave package and strapping arrangement, the influence of the parasitic components, L_S and C_p, is negligible and does not affect the interpretation of the R_S measurement.

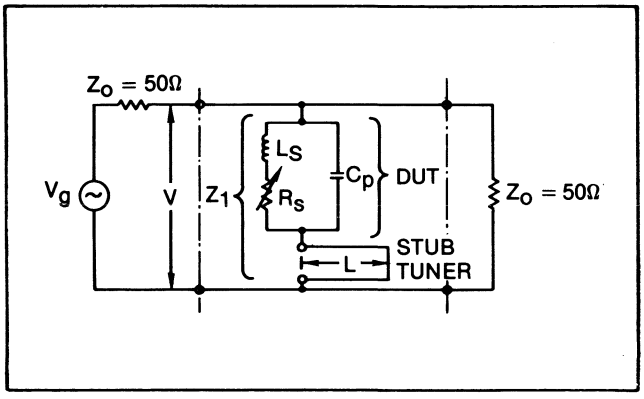


FIGURE 5.2-2 EQUIVALENT CIRCUIT

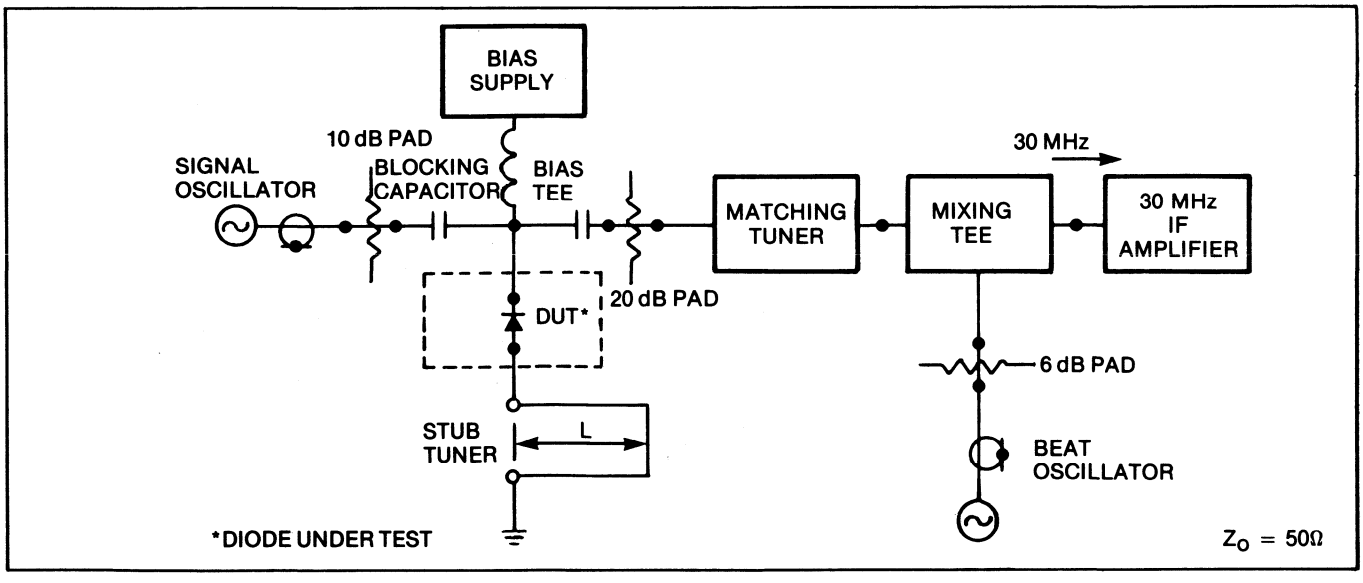


FIGURE 5.2-1 R_S TEST SET

50

By definition:

$$T_V = \frac{V}{V'} \qquad (5\text{-}1)$$

Where T_V = Voltage transmission-loss ratio

V = Voltage across the DUT when the stub tuner is adjusted for maximum transmission to the load.

V' = Voltage across the DUT when the stub tuner is adjusted for minimum transmission to the load.

If the length of the stub tuner, L, in Figure 5.2-2 is adjusted to approximately λ/4, the entire circuit

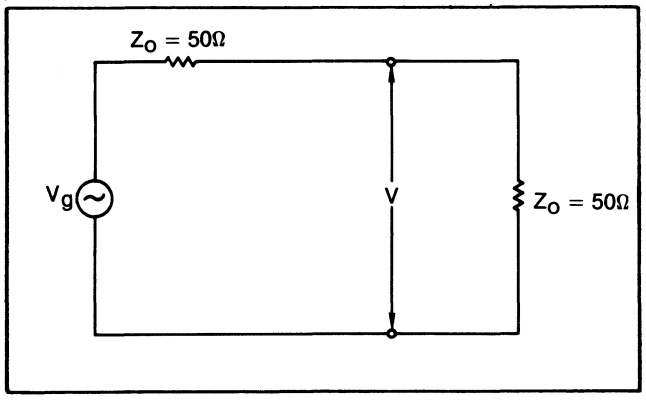


FIGURE 5.3-2 SIMPLIFIED MAXIMUM TRANSMISSION CIRCUIT

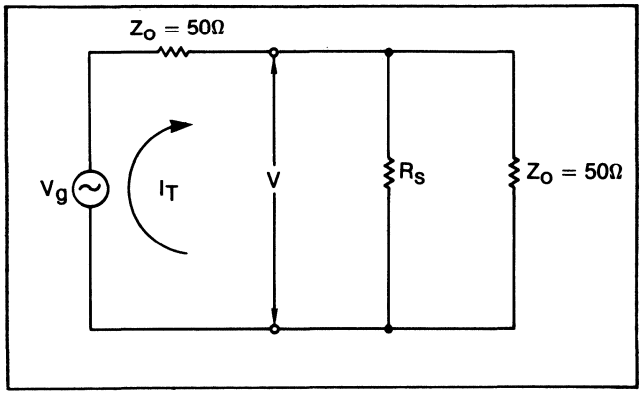


FIGURE 5.2-4 SIMPLIFIED MINIMUM TRANSMISSION CIRCUIT

branch, Z_1, will have a high impedance relative to Z_o and power transfer to the load will be maximum. Figure 5.2-2 will then simplify to Figure 5.2-3.

and:

$$V = \frac{V_g}{2} \qquad (5\text{-}2)$$

Substituting into Equation (5-1):

$$T_V = \frac{V_g}{(2)V'} \qquad (5\text{-}3)$$

If, however, the stub in Figure 5.2-2 is adjusted for minimum power transfer to the load, the imaginary part of the diode impedance will be cancelled and Z_1 will be real. The circuit will be reduced as shown in Figure 5.2-4 (left).

and:

$$I_T = \frac{V_g}{50 + \frac{(50)(R_S)}{50 + R_S}} \qquad (5\text{-}4)$$

It follows that:

$$V' = \left(\frac{V_g}{50 + \frac{(50)(R_S)}{50 + R_S}}\right)\left(\frac{(50)(R_S)}{50 + R_S}\right)$$

Simplifying:

$$V' = \frac{(V_g)(R_S)}{(2)(R_S) + 50} \qquad (5\text{-}5)$$

Substituting into Equation 5-3:

$$T_V = \frac{V_g}{\left(\frac{(2)(V_g)(R_S)}{(2)(R_S) + 50}\right)} \qquad (5\text{-}6)$$

Simplifying:

$$T_V = \frac{R_S + 25}{R_S} \qquad (5\text{-}7)$$

Solving for R_S:

$$R_S = \frac{25}{T_V - 1} \qquad (5\text{-}8)$$

The nomograph of Figure 5.2-5 is useful for solving Equation (5-8).

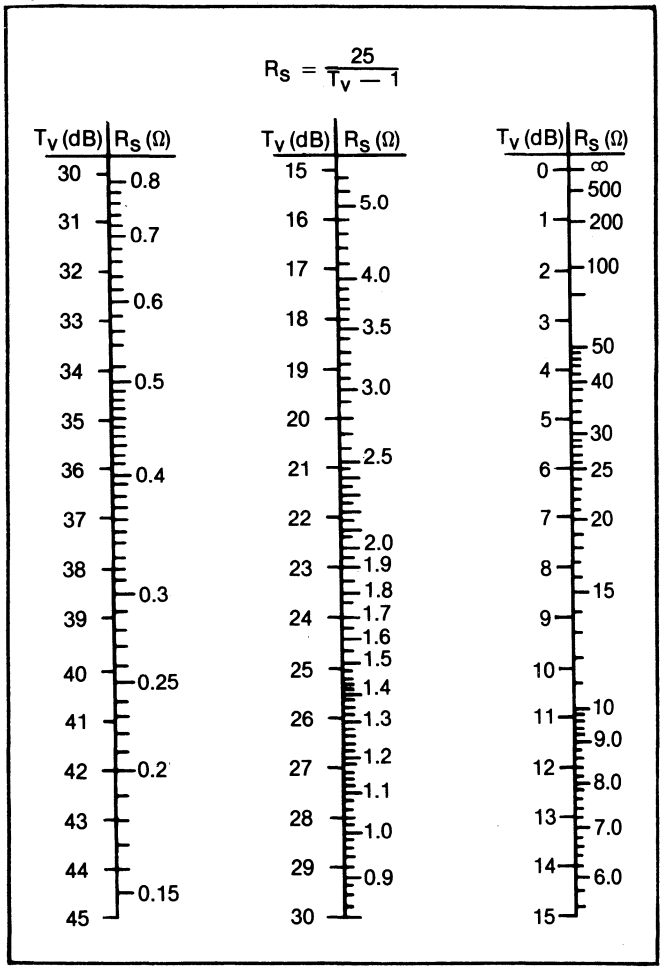


FIGURE 5.2-5 NOMOGRAPH FOR R_S TEST SET

Care should be taken in the design of the diode circuit holder. Reflections and losses contributed by the holder must be accounted for, so that they do not influence the measured value of R_S in the DUT. A good method of checking holder losses is to replace the DUT with a silver-plated slug of the same geometry and then remeasure the voltage transmission-loss ratio. It is desirable to have the transmission-loss ratio of the holder greater than 40 dB.

Thus, with the aid of the nomograph and some care in holder design and maintenance, the R_S test set described herein can provide an accurate, production oriented method for measuring the series resistance of PIN and NIP diodes.

5.3 CARRIER LIFETIME (τ_L)

Carrier lifetime is a measure of a PIN's ability to store charge. Defined in another manner, it is a measure of the delay before an average electron and hole recombine. A pure silicon crystal has a theoretical lifetime of several milliseconds. However, impurity doping can quickly reduce the effective lifetime to microseconds or nanoseconds. Actual measurement of the "average" carrier lifetime is accomplished by injecting a known amount of charge into the I-region of the DUT and measuring the time required to extract it using a reverse bias current. The test set used for performing this measurement is shown in Figure 5.3-1. In measuring the "average" lifetime, the DUT is mounted in series with a 50 ohm transmission line and biased to 10 mA in the forward direction. It is then pulsed negatively. The negative pulse is adjusted so that a peak current of 6 mA flows through the diode in the reverse direction. (See Figure 5.3-2.) The actual pulse applied should have a rapid rise time and its width should be at least several times as long as the expected carrier lifetime. As recombination occurs, the diode charge is depleted. The time period between the start of the negative pulse and the point where it decays to within 10% of its peak-amplitude zero-current level (known as "the 90% point") is defined as the "average" carrier lifetime. Some definitions of carrier lifetime use the 50% point rather than 90% as the interval definition.

5.4 REVERSE RECOVERY (T_{rr})

The reverse recovery measurement is similar to the carrier lifetime measurement in that it evaluates the PIN's ability to store charge (carrier lifetime can in fact be called a special case of reverse recovery time). The distinction in the reverse recovery measurement is that the known charge that we inject into the I-region is swept out by a **large** pulse with an extremely fast rise time, typical of many practical control applications where a fast driving pulse is employed. A typical T_{rr} test set is shown in Figure 5.4-1. The DUT is mounted in series with a 50 ohm transmission line and initially biased to 20 mA in the forward direction. A reverse pulse with a rise time of only 0.25 ns is adjusted for an amplitude 10 times that of the forward-bias level (in this case, 200 mA). The delay cable shown in the circuit block diagram is adjusted for convenience of viewing on the monitoring oscilloscope and takes the place of the pulse advance and delay control on pulse generators with slower rise times. The pulse width cable is a length of open circuited 50 ohm transmission line adjusted to provide a pulse width of $\cong$10 times the expected T_{rr}.

PIN measurements

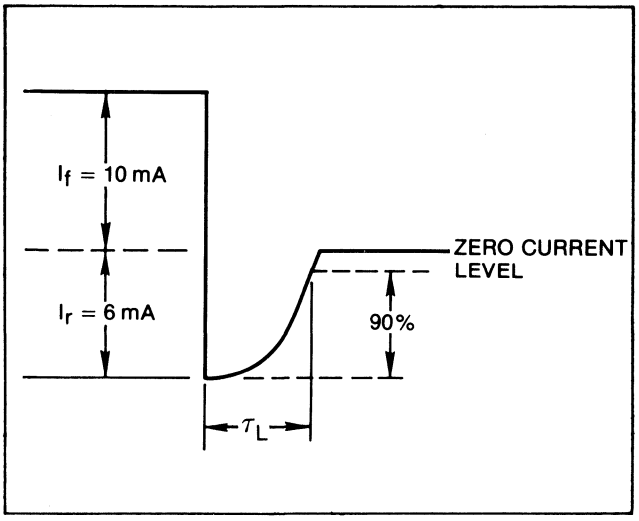


FIGURE 5.3-2 CARRIER LIFETIME PULSE MEASUREMENT

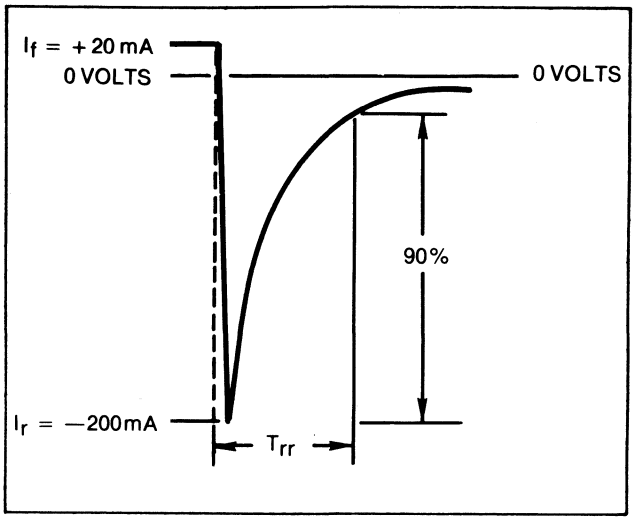


FIGURE 5.4-2 REVERSE RECOVERY TIME WAVEFORMS

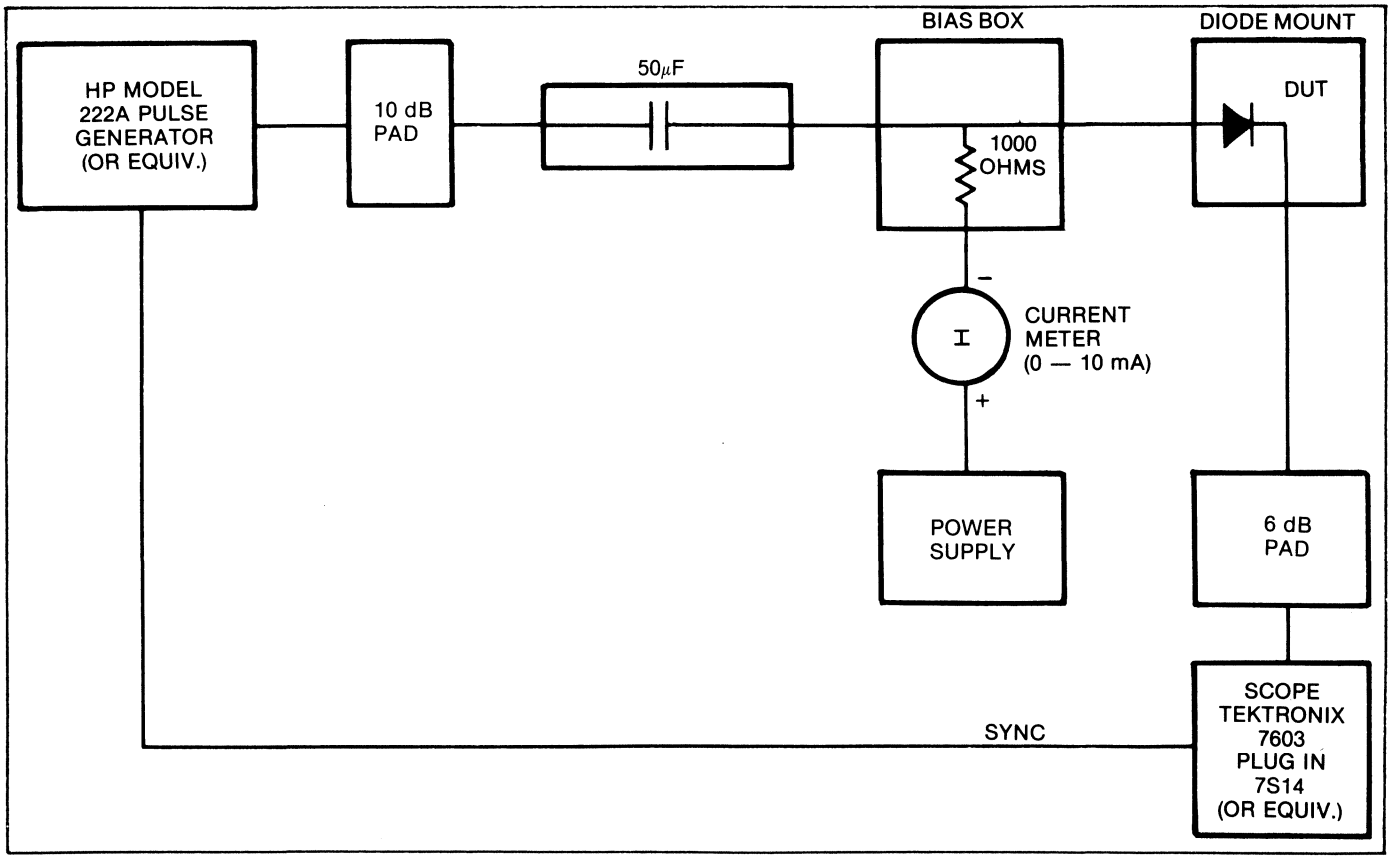


FIGURE 5.3-1 CARRIER LIFETIME TEST SET

The determination of T_{rr} is shown in Figure 5.4-2. As holes and electrons recombine after the application of the 200 mA pulse, the net charge stored in the I-region of the PIN is depleted. The time period between the application of the pulse and the point of 90% depletion is defined as reverse recovery time. As with τ_L, other definitions of T_{rr} relate to the point of 50% depletion.

5.5 THERMAL RESISTANCE (θ_{jc})

Thermal resistance is a measure of a diode's ability to withstand heating effects due to both RF and dc power dissipation. It is defined as the ratio of steady state temperature rise (°C) of the junction per watt of steady state power dissipated within it. (Thermal resistance of unpackaged diodes can be evaluated only on a sample basis with representative devices mounted in appropriate diode enclosures.)

The thermal resistance measurement is achieved by dissipating a known amount of DC power in the DUT and by using the device's voltage variation at a constant forward current of 1 mA as a "calibrated thermometer" to measure the resulting temperature rise. (The change in forward voltage drop with varying temperature is initially determined for each diode type at a constant current of 1 mA in a carefully controlled and monitored oven.) A typical thermal resistance test set is shown in Figure 5.5-1. As shown in Figure 5.5-2 and 5.5-3, the diode's forward voltage is constant as long as the heating current is maintained. The applied heat causes the diode's current-voltage curve to move in. The instant the heating current is pulsed off, the diode's forward voltage drops drastically to a value lower than the 1 mA, room ambient reference. This is due to thermal inertia keeping the diode junction hot, and for an instant, operation is still on the current-voltage curve that was moved in by the applied heat. As the diode cools while the heating current remains off, the forward voltage increases toward the 1 mA room ambient reference, which it never reaches because of the relatively short "OFF" time of the heating pulse.

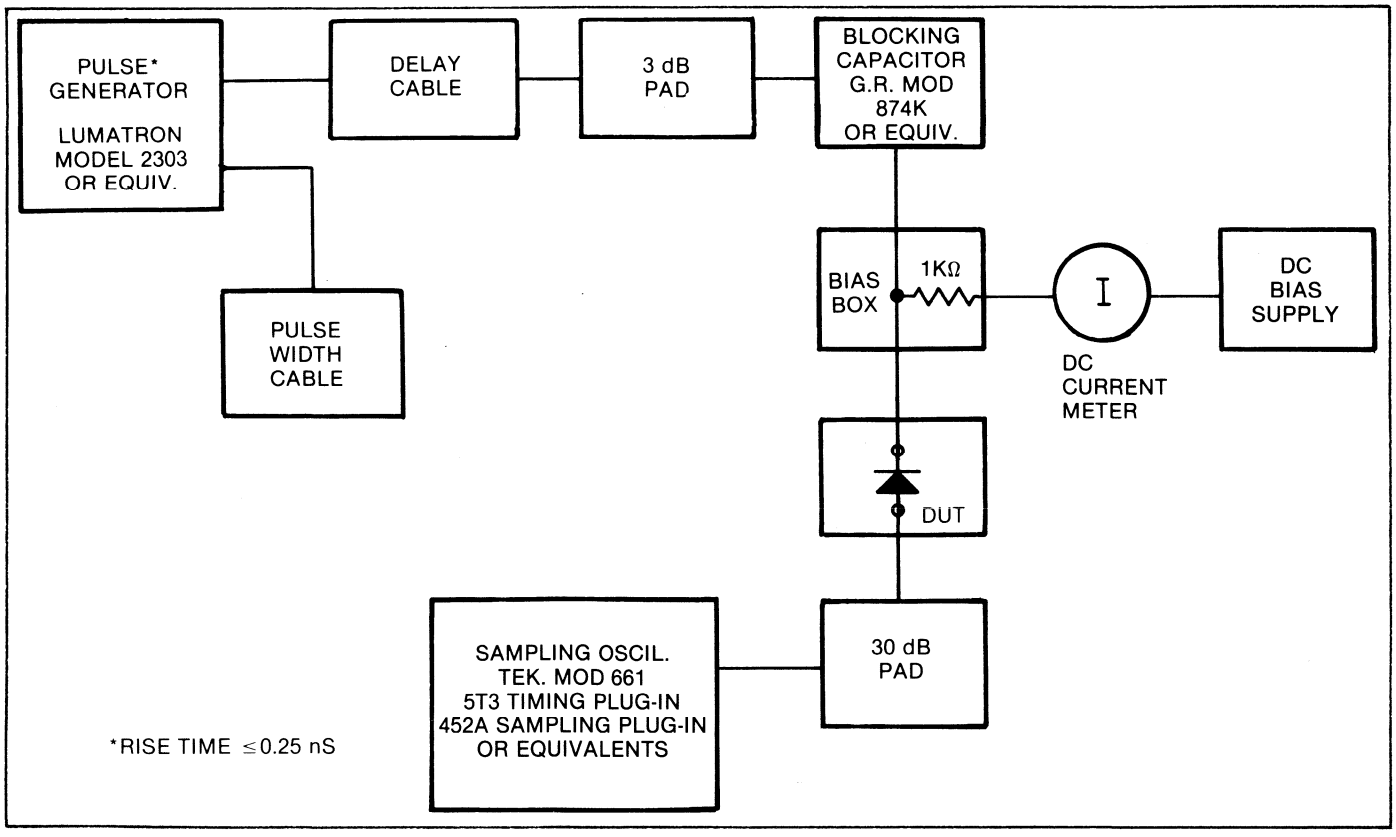


FIGURE 5.4-1 REVERSE RECOVERY TIME TEST SET

The duty cycle of the heating pulse is set at 95%. ΔV, (as shown in Figure 5.5-2), is defined as the voltage difference between the 1 mA room temperature reference and the forward voltage on the diode the instant after the heating current is pulsed off. ΔV is related to the increase in junction temperature that occured while the heating current was on, from our initial "calibration" of forward voltage thermal behavior. Using this information as well as the heating current and diode voltage, thermal resistance is calculated by:

$$\theta_{jc}\,(°C/W) = \frac{\Delta T\,(°C)}{(E)\,(I_{HT})} \qquad (5\text{-}9)$$

where:

θ_{jc} = device thermal resistance (in °C/W)
ΔT = temperature rise as determined from ΔV and previous oven calibration data (in °C)
E = voltage across DUT during applied heating current (in volts).

The maximum power dissipation for an M/A diode of known thermal resistance at various ambient temperature, is determined from the curves of Figure 2.9-4.

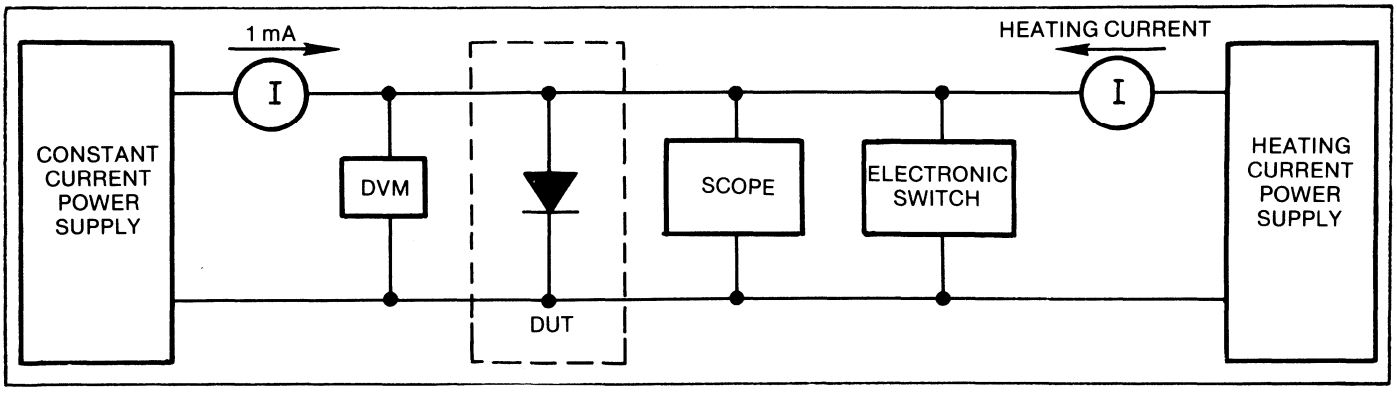


FIGURE 5.5-1 THERMAL RESISTANCE TEST SET

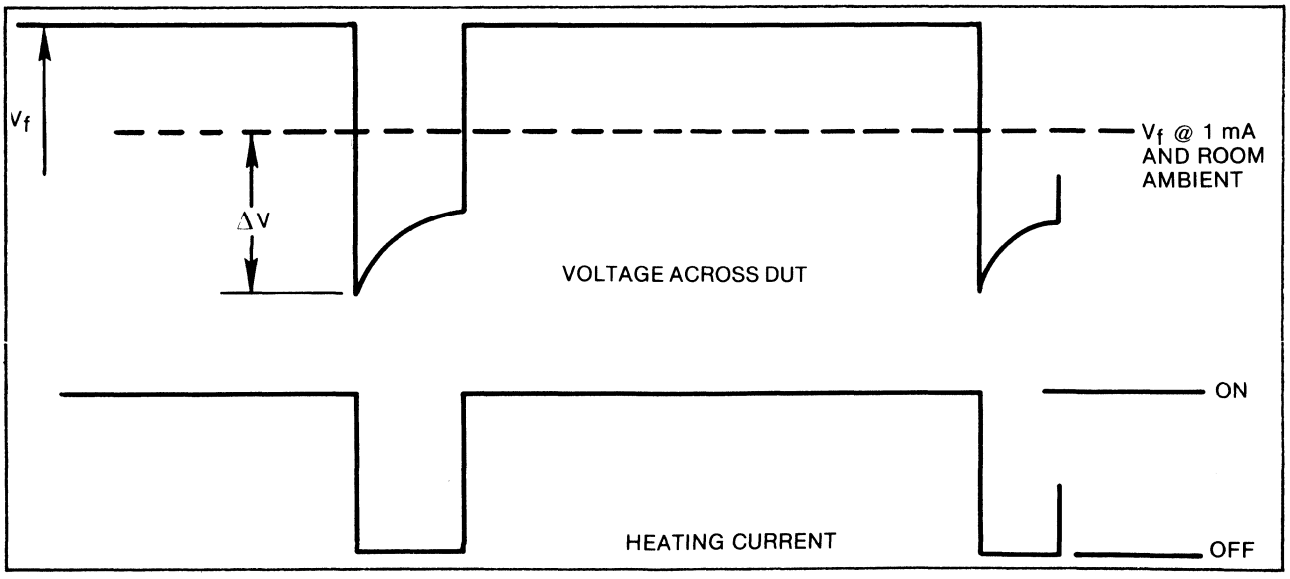


FIGURE 5.5-2 THERMAL RESISTANCE PULSE FORM

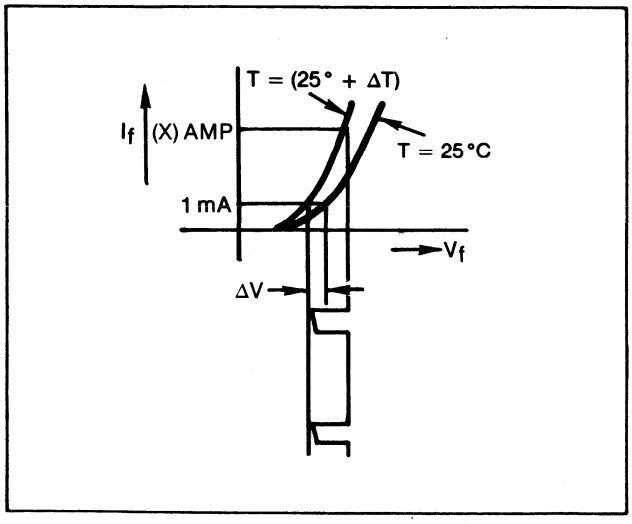


FIGURE 5.5-3 CHANGING FORWARD VOLTAGE WITH APPLIED HEATING CURRENT

package parasitics for specific M/A case styles

package parasitics for specific M/A case styles

6.1 DISCUSSION

In both chapters 2 and 10, switch performance is considered using diodes or packaged diodes with parasitics tuned out. This section will show how to determine the electrical value of the external tuning components and how to realize them in a relatively narrowband circuit.

Figure 6.1-1 shows the complete schematic for a PIN diode as well as the electrical components necessary to tune out the device parasitics, lead inductance (L_S) and case capacitance (C_P).

Failing to tune out case parasitics results in effects which become dramatic as frequency increases. Section 2.12 analyzed the actual electrical performance of three multi-throw switches which use packaged PIN diodes with untuned parasitics. Figure 6.1-1 shows L_{ext} used to parallel-resonate the capacitance of the device enclosure. This resonance provides a very high and therefore negligible impedance in shunt with the R_S, C_j and L_S series combination. L_{ext} can be realized if a stub or branch line, of critical length and spacing from the diode, is inserted into the circuitry. C_{ext} is used to series-resonate the lead inductance. This resonance provides a very low, and therefore negligible impedance. C_{ext} can be realized if a critical TEM line length is placed in series with the packaged diode. It is recommended that both L_{ext} and C_{ext} be somewhat variable to account for tolerances in package parasitics.

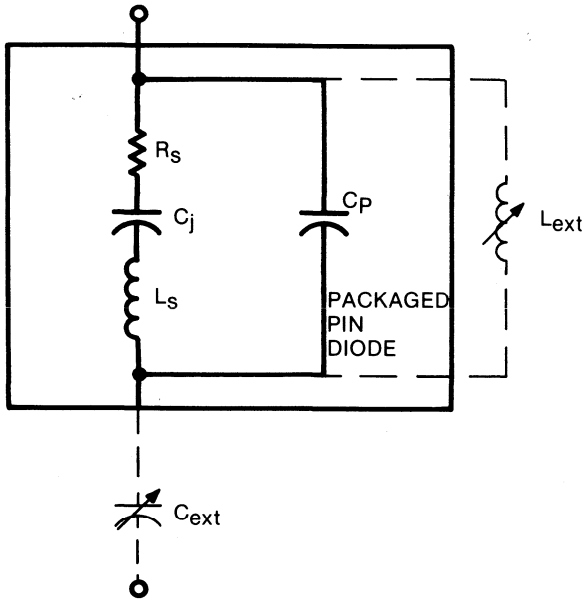


FIGURE 6.1-1 EQUIVALENT CIRCUIT OF A PACKAGED PIN DIODE WITH EXTERNAL TUNING

The value of C_{ext} is calculated from the formula:

$$C_{ext} = \left(\frac{1}{2\pi F\, L_S}\right)^2 (L_S) \qquad (6\text{-}1)$$

The value of L_{ext} is calculated from the formula:

$$L_{ext} = \left(\frac{1}{2\pi F\, C_p}\right)^2 (C_p) \qquad (6\text{-}2)$$

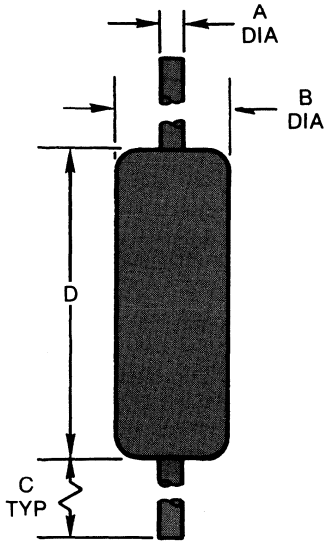
In the above formulas, F is the frequency of operation, L_S is the series inductance attributed mainly to the diode connecting strap, and C_p is the package capacitance.

6.2 PACKAGE PARASITICS FOR SPECIFIC M/A CASE STYLES

For each standard MA PIN case style illustrated in this section, the physical dimensions are tabulated. The parasitics C_p and L_S are defined, and the external parameters C_{ext} and L_{ext} necessary to tune them out are shown in graph form.

package parasitics for specific M/A case styles

4



DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.018	0.022	0,46	0,56
B	0.085	0.107	2,16	2,72
C	1.000	— —	25,40	— —
D	0.230	0.300	5,84	7,62

FIGURE 6.2-1a. CASE STYLE 4 — OUTLINE DRAWING

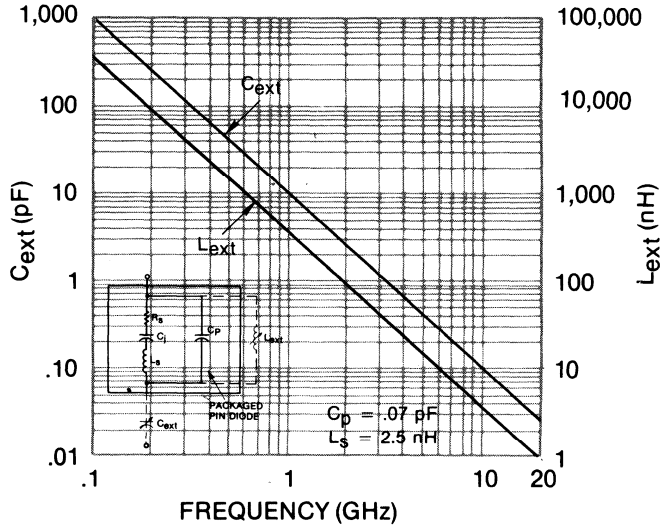
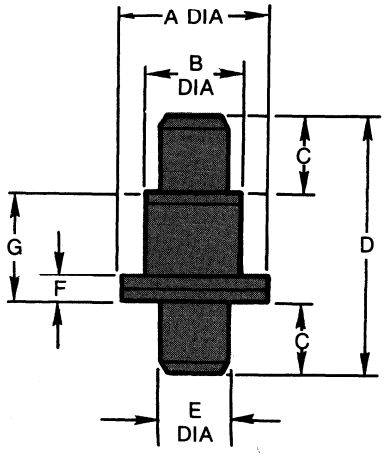


FIGURE 6.2-1b CASE STYLE 4 — VALUES OF EXTERNAL PARAMETERS NECESSARY FOR RESONATING CASE PARASITICS

30



DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.119	0.127	3,02	3,23
B	0.079	0.083	2,01	2,11
C	0.060	0.064	1,52	1,63
D	0.205	0.225	5,21	5,72
E	0.060	0.064	1,52	1,63
F	0.016	0.024	0,41	0,61
G	0.085	0.097	2,16	2,46

FIGURE 6.2-2a. CASE STYLE 30 — OUTLINE DRAWING

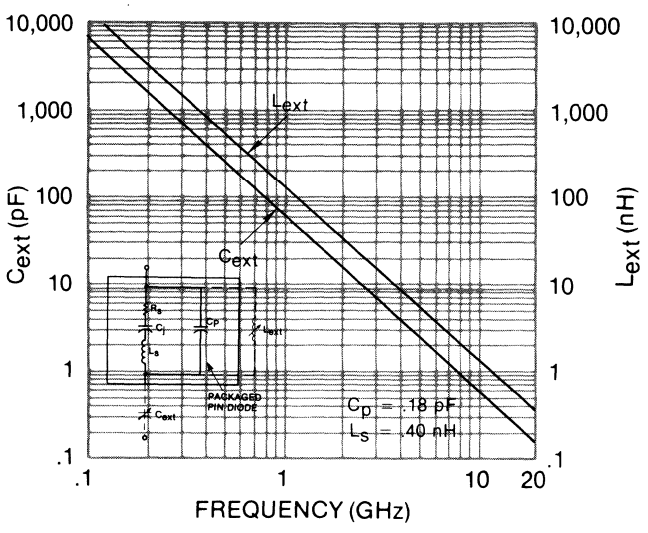
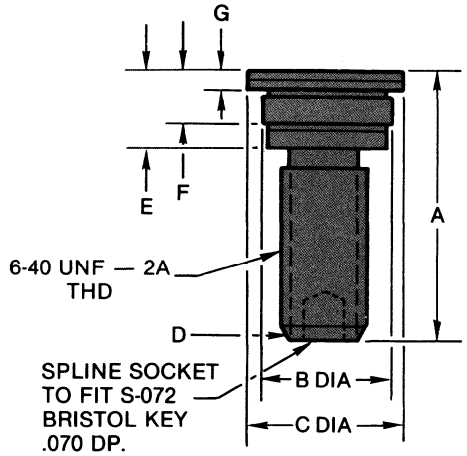


FIGURE 6.2-2b CASE STYLE 30 — VALUES OF EXTERNAL PARAMETERS NECESSARY FOR RESONATING CASE PARASITICS

package parasitics for specific M/A case styles

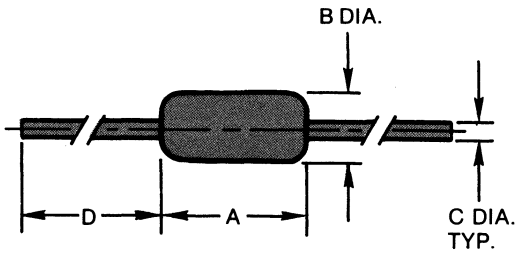
43



DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.440	0.460	11,18	11,68
B	0.208	0.212	5,28	5,38
C	0.255	0.265	6,48	6,73
D	.020 X 45° REF.		0,51 X 45° REF.	
E	0.119	0.131	3,02	3,33
F	0.050 REF.		1,27 REF.	
G	0.025	0.035	0,64	0,89

FIGURE 6.2-3a. CASE STYLE 43 — OUTLINE DRAWING

54



DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.145	0.165	3,68	4,19
B	0.068	0.075	1,72	1,91
C	0.014	0.016	0,35	0,41
D	1.000	1.500	25,40	38,10

FIGURE 6.2-4a. CASE STYLE 54 — OUTLINE DRAWING

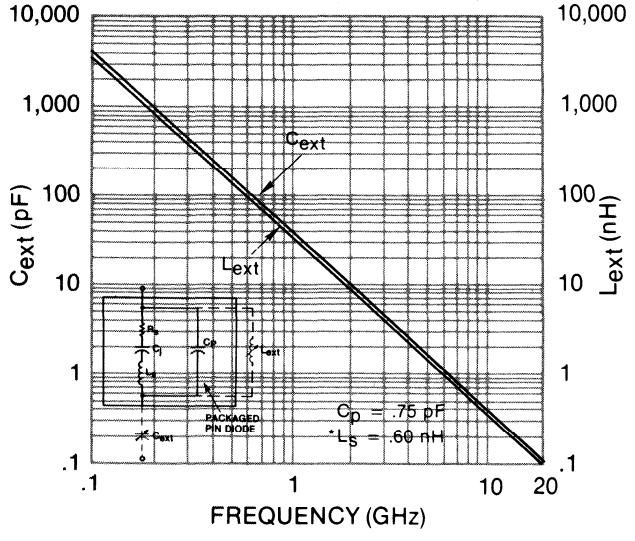


FIGURE 6.2-3b CASE STYLE 43 — VALUES OF EXTERNAL PARAMETERS NECESSARY FOR RESONATING CASE PARASITICS

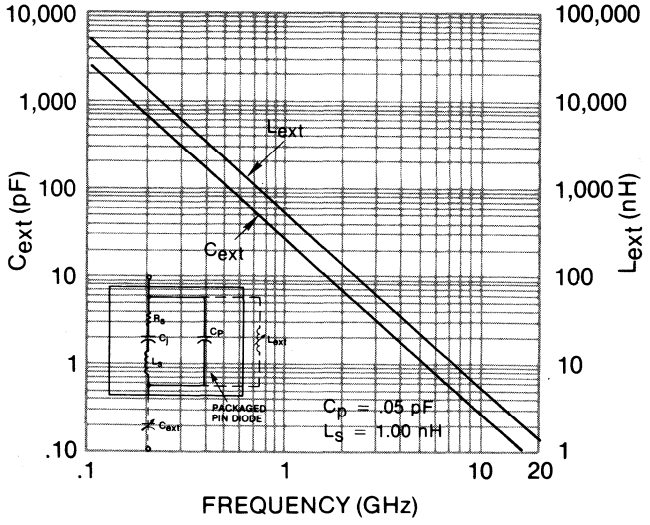
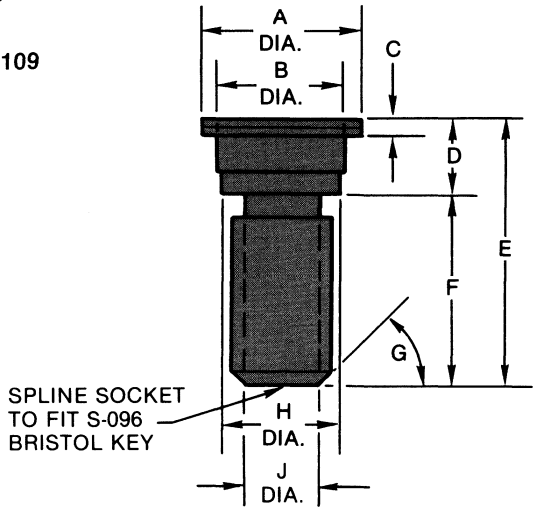


FIGURE 6.2-4b CASE STYLE 54 — VALUES OF EXTERNAL PARAMETERS NECESSARY FOR RESONATING CASE PARASITICS

package parasitics for specific M/A case styles

109



DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.259	0.267	6,58	6,78
B	0.207	0.213	5,26	5,41
C	0.027	0.033	0,69	0,84
D	0.118	0.134	3,00	3,40
E	0.446 REF.		11,33 REF.	
F	0.317	0.323	8,05	8,20
G	40°	50°	40°	50°
H	0.193	0.199	4,90	5,05
J	0.110	0.130	2,79	3,30

FIGURE 6.2-5a. CASE STYLE 109 — OUTLINE DRAWING

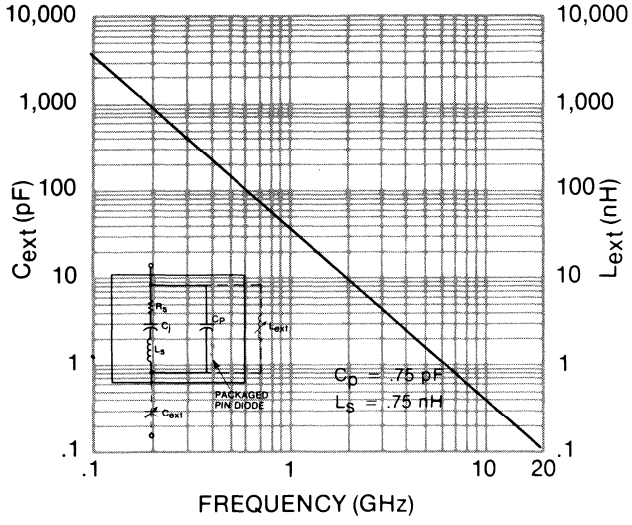
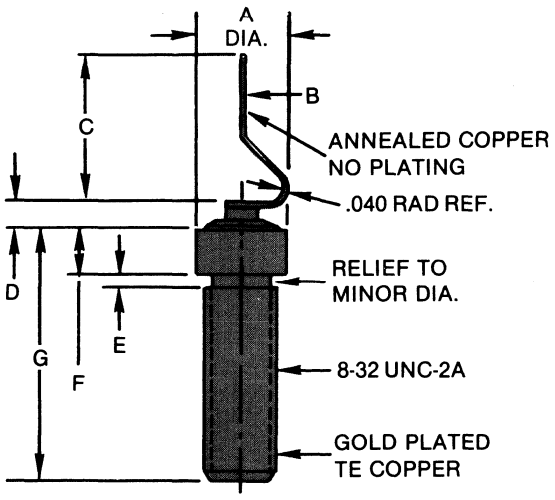


FIGURE 6.2-5b CASE STYLE 109 — VALUES OF EXTERNAL PARAMETERS NECESSARY FOR RESONATING CASE PARAMETERS

150



DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.180	0.190	4,57	4,83
B	0.070	0.110	1,78	2,79
C	0.300	0.360	7,80	9,10
D	0.048 REF.		1,22 REF.	
E	0.020	0.040	0,51	1,02
F	0.095	0.105	2,41	2,67
G	0.730	0.770	18,54	19,56

FIGURE 6.2-6a. CASE STYLE 150 — OUTLINE DRAWING

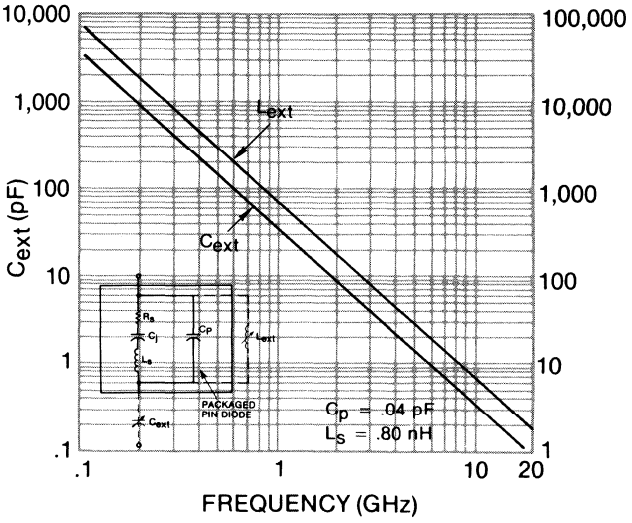


FIGURE 6.2-6b. CASE STYLE 150 — VALUES OF EXTERNAL PARAMETERS NECESSARY FOR RESONATING CASE PARASITICS

quality and reliability

quality and reliability

"THE POLICY OF MICROWAVE ASSOCIATES IS THAT ITS PRODUCTS SHALL BE DELIVERED TO ITS CUSTOMERS ON SCHEDULE AND AT A COMPETITIVE PRICE, AND SHALL MEET ALL SPECIFIED AND IMPLIED STANDARDS OF PERFORMANCE, RELIABILITY AND QUALITY."

MICROWAVE ASSOCIATES CORPORATE POLICY CP-12

7.1 DISCUSSION

This section will discuss the reliability of Microwave Associates' PIN diodes, how reliability of a diode is defined, tested and demonstrated, and what this reliability means to the user of PIN diodes. Prior to any reliability discussion, however, a review of key diode processing features, quality control and electrical-environmental screening is necessary.

7.2 KEY PROCESSING FEATURES

The processes involved in fabrication of a PIN diode which have the greatest effect upon reliability are those of metallization and passivation. With the advent of gold metal systems used in conjunction with appropriate barrier metals such as titanium-tungsten, the incidence of failures under normal operating temperatures has greatly decreased and is no longer a significant failure mechanism in high reliability (hi-rel) diodes. All PIN diodes manufactured by Microwave Associates use gold metallization schemes exclusively. The technology of passivation is a result of rigorous attention by the semiconductor industry to the minimization of oxide charge-drift and contamination during wafer processing. Thus, only a few high technology semiconductor suppliers such as Microwave Associates can offer devices with MTBF's in excess of 10^6 hours. The preferred passivations are silicon dioxide and silicon nitride. Although neither is hermetic, each provides excellent characteristics for hi-rel diodes. To achieve hi-rel status, the passivated chips must be assembled into hermetic packages. These packages have long been used in conventional microwave components.

In recent years, hybrid microwave integrated circuits have become more and more popular due to advantages in cost, weight, size and circuit complexity. This trend accelerates the need for PIN diodes in chip form, but at the same time places more stringent requirements on the PIN diode chip. The larger circuit assembly is less likely to be hermetic and, due to increased chip handling, the likelihood of mechanical damage to the chip is greatly increased.

To meet these more stringent requirements Microwave Associates offers its hermetic CERMACHIP™ passivation on selected PIN diode types MA-4P504 through MA-4P709.

A CERMACHIP™ PIN diode is a mesa diode passivated with a continuous hard, thick glass layer over its entire active area. This hard glass passivation totally protects the diode junction from environmental comtamination because of the absence of the pinholes and other voids which are found in the more common silicon dioxide and silicon nitride passivation systems. Also, the hardness and thickness (approximately 40 times thicker than silicon dioxide layers) of the glass greatly reduces the diode's susceptibility to mechanical damage. The CERMACHIP™ PIN diode is as hermetic as any conventional ceramic or glass package, with the obvious advantage of being considerably smaller in size.

In summary, CERMACHIP™ PIN diodes are uniquely useful not only in applications where high reliability products are required in a non-hermetic environment, but they also offer unparalleled reliability performance in high power hermetic circuit environments.

7.3 QUALITY CONTROL

The Quality Control function at Microwave Associates is one of total involvement in the design, development, manufacturing and reliability assurance of our semiconductor devices. The key responsibilities of M/A Quality Control are:

1) Incoming inspection of all purchased materials to documented specifications.

2) Calibration of manufacturing test equipment on a regular basis against known standards.

3) Q.C. in-line inspection of product at various key steps during the manufacturing process as shown in the process flow diagram of Figure 7.3-1.

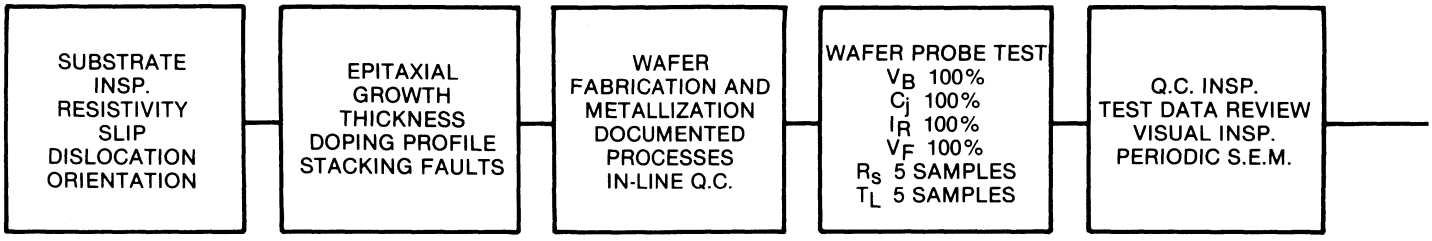
4) Performance of all electrical and environmental screening, Group B testing, Group C testing and other reliability tests per the appropriate MIL-STD procedures or customer specification.

5) Final inspection of product to customer specification prior to shipment.

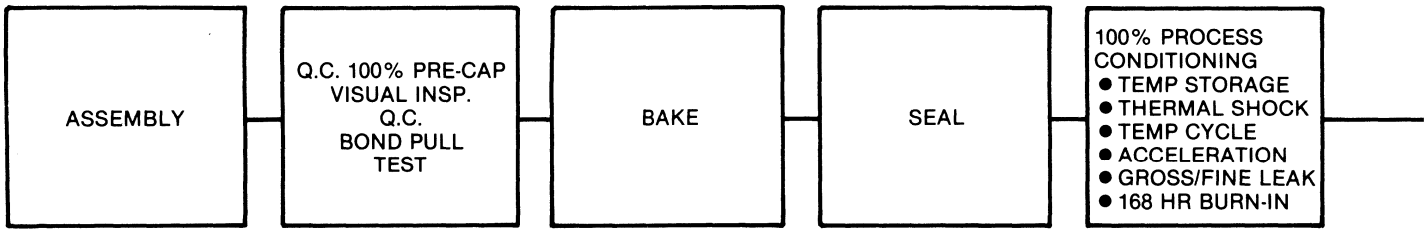
6) Responsibility for introduction, maintenance, review and adherence to documented specifications for all processes in the manufacture of Microwave Associates' semiconductors.

quality and reliability

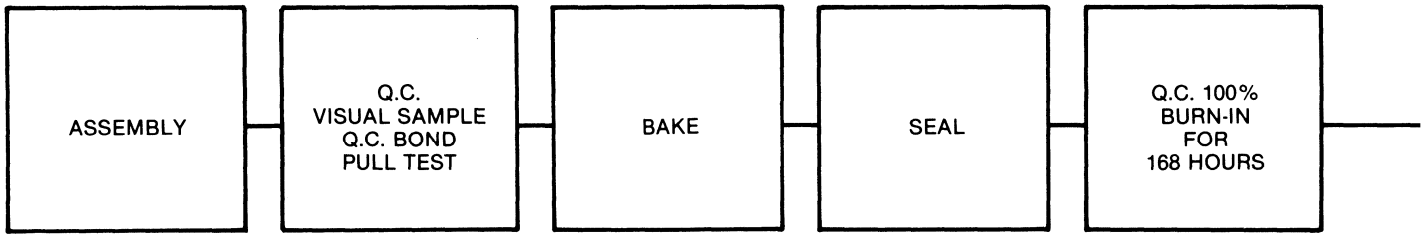
WAFER PREP



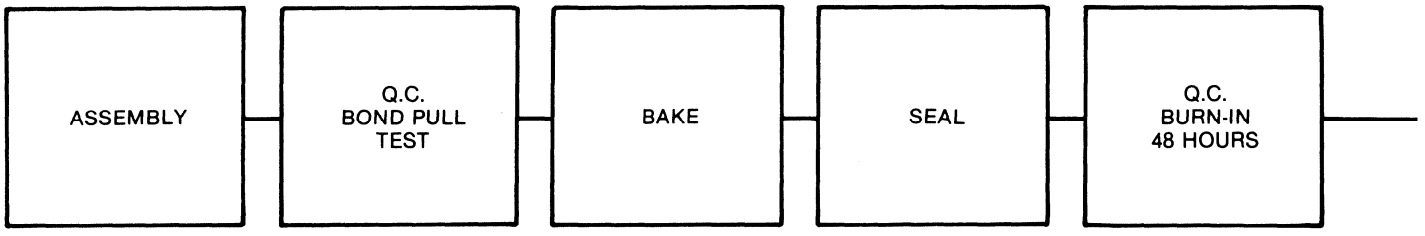
JANTX JANTXV LEVEL (PACKAGED)



JAN LEVEL (PACKAGED)



INDUSTRIAL LEVEL (PACKAGED)



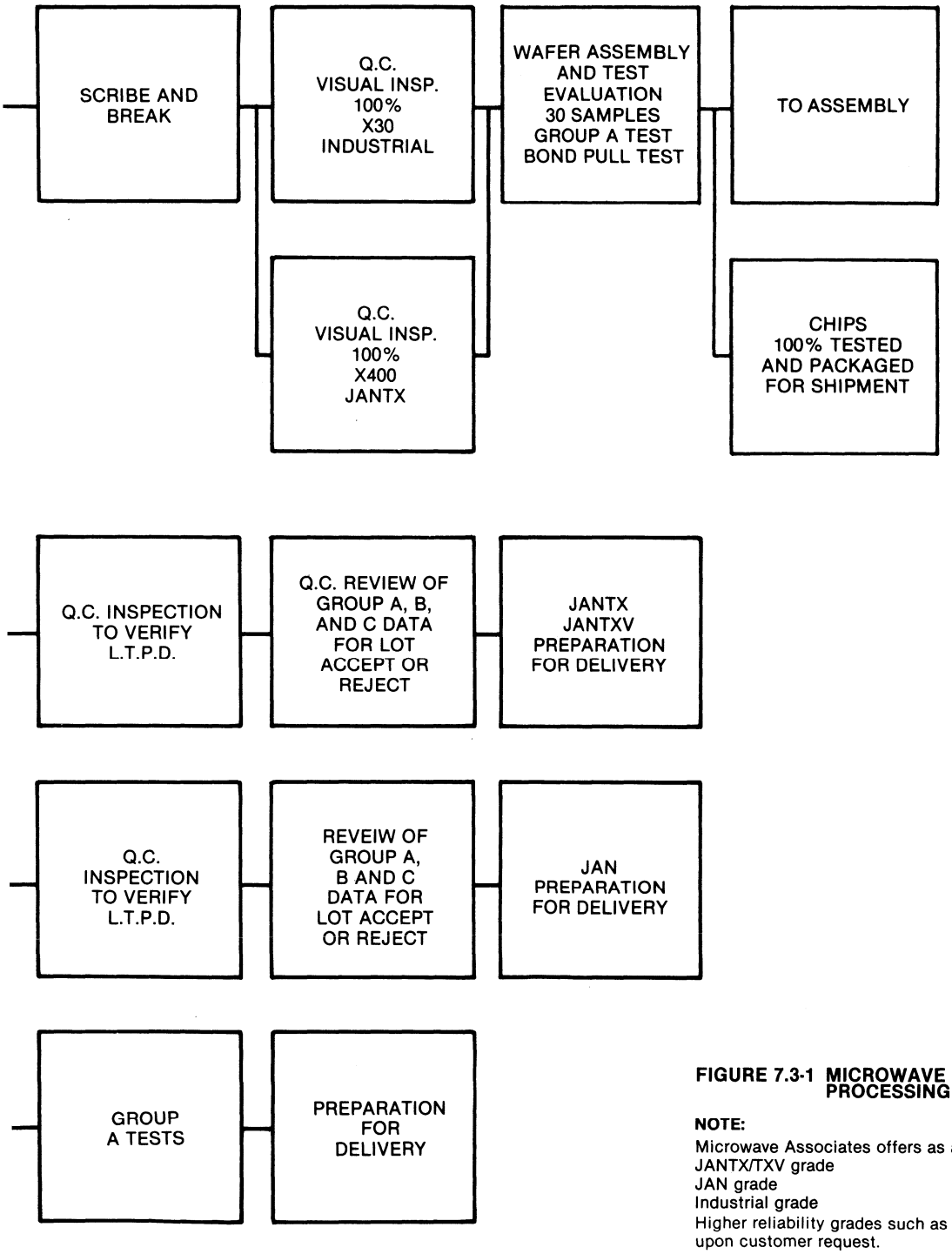


FIGURE 7.3-1 MICROWAVE ASSOCIATES PIN DIODE PROCESSING SEQUENCES

NOTE:
Microwave Associates offers as a standard, three reliability grades
JANTX/TXV grade
JAN grade
Industrial grade
Higher reliability grades such as JANS or equivalent are offered upon customer request.

quality and reliability

Microwave Associates welcomes a customer review of our quality control procedures.

7.4 ELECTRICAL AND ENVIRONMENTAL SCREENING

While all Microwave Associates' PIN diodes are routinely manufactured as "hi-rel" semiconductors, it is recommended for applications where reliability is a primary criterion, that an electrical and environmental screening of the diodes be performed to eliminate any early failures.

A suggested screening program for PIN diodes to JANTX level is listed in Table 7-A. This program can be supported by Group B sampling for compliance to JANTXB or JANTXVB as shown in Table 7-B.

Customer requests for additional or alternate testing programs can be complied with, as can customer requests for reliability levels above JANTX status such as JANS or equivalent.

7.5 RELIABILITY

Product reliability is the culmination of a carefully planned design, development and manufacturing effort using the most up-to-date proven processing techniques. It is no surprise to any one familiar with microwave semiconductors that only the most technologically advanced companies are able to consistently produce the devices required to achieve the reliability levels demanded by today's system requirements.

Reliability is defined as the probability of a device performing its purpose adequately for the period of time intended under the operating conditions

TABLE 7-A MIL-STD-750 TYPICAL 100% PRECONDITIONING AND SCREENING PROGRAM FOR TX LEVEL SCREENING

Inspection	Method	Condition
Internal Visual	2072/	See Note 2
and/or X-Ray	2076	— —
High Temperature Life	1032	48 hrs min at max. storage temp.
Thermal Shock	1051	10 cycles
Constant Acceleration	2006	20,000 g, Y_1
Fine Leak	1071	H
Gross Leak	1071	C or E
Electrical	— —	See Note 3
Burn-in	1038	See Note 3
Electrical	— —	See Note 3
Stability Verification	— —	See Note 3

NOTES:

1. Inspection plan shown is for packaged diodes. Screening plans for chip diodes available on request.
2. Internal visual on TXV and TXVB screening programs only. X-ray is optional for any screening plan.
3. Conditions and detail tests depend on specific part number. Information available on request.

TABLE 7-B MIL-STD-750 TYPICAL SAMPLING PROGRAM FOR TXB OR TXVB PARTS

Inspection	Method	Condition	LTPD
Subgroup 1			
Physical Dimensions	2066	— —	10-20
Subgroup 2			
Solderability	2026		
Thermal Shock	1051	10 cycles	10-20
Thermal Shock	1056	A	
Hermetic Seal	1071	Condition H, C or E	
Moisture Resistance	1021		
Electrical	— —	See Note 2	
Subgroup 3			
Shock	2016	1500 g, ½ms, 5 x @ X, Y_1Y_2	
Vibration, Variable freq.	2056		
Constant Acceleration	2006	20,000 g @ X, Y_1Y_2	10-20
Electrical	— —	See Note 2	
Subgroup 4			
Terminal Strength	2036	E	10-20
Subgroup 5			
High Temperature Life	1031	Max. storage temp.	$\lambda = 5$
Electrical	— —	See Note 2	
Subgroup 6			
Operating Life	1026	See Note 2	$\lambda = 5$
Electrical	— —	See Note 2	

NOTES:

1. Test plan is for packaged diodes. Programs for chips are available on request.
2. Conditions and detail tests depend on specific part numbers. Information available on request.

encountered. Notice that three factors are needed to define reliability:

1) Probability of survival

2) Operating time period

3) Operating conditions

All three are expressed as precise numerical quantities, and a statement of reliability that omits any one of the three factors is of no value to the user. **Thus, a statement that a part exhibits a failure rate of 10 FITS is meaningless unless the operating temperature and conditions are defined.** (1 FIT is the failure rate if 1 failure occurs in 10^9 device hours of operation. A device hour can be obtained in any number of ways. It is one device operating for one hour, or two devices operating for ½ hour, etc.)

It is also important to note that a product which is of high quality may not have a high degree of reliability. However, a product which has a high degree of reliability must be of high quality. Microwave Associates provides both high quality and high reliability.

For a single component series system (a system that fails if one component fails), a plot of system failure rate will be identical to the component failure rate. Figure 7.5-1 shows a typical failure rate curve, applicable to any semiconductor device. Initially, the failure rate is higher than allowed by system design and is called the "early failure period". These early failures are due to defects introduced in the manufacturing process which remain undetected despite the implementation of stringent processing controls.

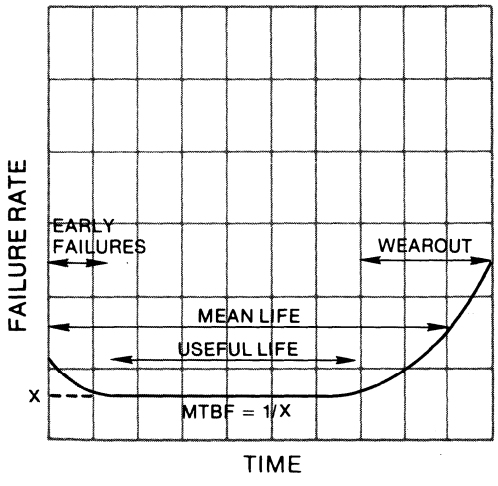


FIGURE 7.5-1 PIN FAILURE RATE

The early failures are always brought to an acceptable level before installation in any system, by electrical and environmental screening of finished devices, a process often referred to as "burn-in". After the initial early failure period, the system will settle down and exhibit a constant failure rate, X. Microwave Associates offers burn-in and screening services to eliminate early failures.

The period during which the failure rate is constant is called the "useful life" of the system because it is in this period that the component can be utilized to the greatest advantage. The failures that do occur are called "chance failures". The physical mechanism of such failures is a sudden accumulation of stresses acting on and in the component. To minimize the chance failure rate, it is wise to operate components at specified rated levels which are conservatively chosen.

For example, a PIN diode operating at levels much below its power and temperature ratings will be far less subject to chance failures than a similar device operating close to maximum ratings, where a sudden system perturbation could exceed specified safe operating conditions.

Customer and device manufacturers must jointly evaluate reliability cost trade-offs, the optimum selection of operating conditions and device features which will ensure that the reliability goal is eventually met: virtual elimination of field failures within the intended useful life of the system.

The reliability, R(t), at time, t, in the useful life region is given by:

$$R(t) = e^{-Xt} \qquad (7\text{-}1)$$

where the function R(t) is the probability that the device, which has a constant failure rate, will not fail in the given operating time, t. The mean time between failures, (MTBF) is merely the reciprocal of X:

$$MTBF = \frac{1}{X} \qquad (7\text{-}2)$$

Specifying MTBF is the most common way of expressing a part's reliability, but it must be used with caution. Before it can be applied to a particular situation, it is necessary to estimate the mean life of

the component. The mean life is the time taken to fail half of a given population and includes failures from the wear-out region. (See Figure 7.5-1.) Wear-out occurs at the end of a product's useful life and is a symptom of a component's aging. In most semiconductor circuit applications, the mean life is designed to be much greater than the intended life of the system so that wear-out does not contribute to the failure rate.

To illustrate these concepts, consider purchasing one-hundred-thousand light bulbs. To establish an MTBF rating, each bulb could be simultaneously operated for 100 hours. Suppose 10 failed; the experimentally determined MTBF is:

$$\text{MTBF} = \frac{100{,}000 \times 100}{10} = 10^6 \text{ hours} = 114 \text{ years}$$

which is a very impressive number. However, this does not mean that the bulbs can be operated for 10^6 hours. Their mean life is probably several thousand hours and unless the user clearly understands the difference he may be disappointed after half a year to find out that only half the bulbs are still operational. **MTBF estimates are of no value unless accompanied by an estimate of the parts' mean life.**

If a component exhibits an MTBF of 10^6 hours, it means, using Equation 7-1, that the probability that the device will not fail in any given 10 hour period is 0.99999 or 99.999 percent provided operation is restricted to the useful life period.

The major difference between the useful life period and the wear-out region is that the failure rate, X, is constant for chance failures, whereas it increases rapidly as wearout progresses and the operating time reaches the mean time. Much investigation of this failure region has been performed with the result that characteristic failure mechanisms have been identified and in some cases reduced or eliminated.

TABLE 7-C

MECHANISM	E_a (eV)
Oxide Charge Drift	~1.02
Electromigration • Gold • Aluminum	 ~0.61 ~0.48
Gold Diffusion through Titanium-Tungsten Refractory Metal Barrier	~1.8

For example, the failure rate due to these mechanisms is a strong function of temperature and follows the Arrhenius law:

$$\text{F.R.} = Ae^{\frac{E_a}{kT}} \qquad (7\text{-}3)$$

where:
F.R. = Failure Rate
A = constant
E_a = activation energy (eV)
k = Boltzmann's Constant (joule/°K)
T = temperature (°K)

The mean life of semiconductor devices, whether they be microwave diodes or microwave bipolar transistors, can exceed 10^8 hours (more than 11,000 years) at room temperature, for well designed and thoroughly screened parts. Experiments to study the wearout failure region at room temperature cannot be performed because of this time magnitude. However, if the temperature is raised sufficiently high enough, the failure rate will increase to a measurable level within a reasonable time frame (100 to 10,000 hours). Such testing, called "accelerated" or "step stress" testing, has been used to assess the mean life of many semiconductor devices, despite the implicit assumption that the failing mechanisms are the same at all temperatures. Experimental care and knowledgeable analyses are needed before such extrapolations can be made.

Activation energies have been assigned to various isolated failure mechanisms. These failure mechanisms have been determined by careful physical analysis of failed parts. Three of particular importance to microwave semiconductors are given at left in Table 7-C.

Oxide charge-drift, which leads to leakage current and low frequency parameter drifts, was an early problem with most semiconductor devices. However, the rapid advances made in metal-oxide silicon (MOS) technology were brought about by the ability to control oxide charge-drift through meticulous and clean processing schedules and today's microwave devices fully utilize these technological advances. Seldom, if ever, do they experience this problem and wafers that do are eliminated through the use of screening procedures.

The very high activation energy of the universally used gold refractory metallization system, where diffusion of gold finally penetrates the diffused junc-

tion, means that at normal system operating temperatures (< 175 °C) this mechanism does not contribute to failures.

Finally, the development of the hermetic CERMACHIP™, ideally suited for high power, high reliability system requirements has been demonstrated by RF and dc testing to equal previously attained reliability levels of low power devices.

As a consequence of these technology improvements, thoroughly screened Microwave Associates PIN diodes can meet the MBTF, mean life and FIT reliability levels shown in Table 7-D.

The low power, lower breakdown voltage diodes feature silicon dioxide/silicon nitride passivation and use pure gold contacts with a refractory metal barrier. The passivation failures are insignificant for such devices at reasonable operating temperatures. The refractory metal contact scheme will not fail by diffusion, alloying or cracking until very high temperature-time levels are reached, such as 1.2×10^4 hours at 300 °C. This reliability results in an extremely long mean life for such devices. The low power devices feature very thin p+ diffusion layers for minimum loss. The refractory metal contacts have been developed to provide maximum reliability and mean life for such devices. The curve of mean life versus temperature for low power PIN diodes, types MA-4P101 through MA-4P404 is shown in Figure 7.5-2.

The CERMACHIP™ process was developed to address the needs of higher power, thicker I-region diodes. For this class of diodes, silicon dioxide/silicon nitride passivation is inadequate even in a hermetic sealed package and would be the dominant failure mechanism. However, the CERMACHIP™ process has reduced passivation failures to an insignificant level. The dominant failure mechanism becomes the failure of the nickel gold ohmic contact by diffusion and alloying at large temperature time products, such as 1,000 hours at 250 °C. At normal operating temperatures for PIN diodes, the CERMACHIP™ process exhibits high reliability, and mean life in excess of 10^8 hours. High power devices made with the CERMACHIP™ process have much thicker p+ layers than low power devices. The nickel gold ohmic contact provides excellent low loss and high reliability contacts to this class of high power devices. The curve of mean life versus temperature for the high power CERMACHIP™ diodes, types MA-4P504 through MA-4P709, is also shown in Figure 7.5-2.

TABLE 7-D DEMONSTRATED RELIABILITY LEVEL DATA

POWER RANGE AND DIODE TYPE	MTBF	MEAN-LIFE	F.I.T.[1] LEVEL
A) Low-power[2] PIN diodes MA-4P101 through MA-4P404	$>10^8$ hours	$>10^{10}$ hours	1 — 10 FITS
B) High-power[3] CERMACHIP™ Diodes, MA-4P504 through MA-4P709	$>10^8$ hours	$>10^{10}$ hours	1 — 10 FITS

NOTES:

1. Failures in Time (F.I.T.) 1 FIT is the failure rate, if one diode failure occurs in 10^9 device hours of operation. A device hour can be obtained in any number of ways; it is 1 device operating for 1 hour, or 2 devices operating for ½ hour, etc.
2. This data applies to devices in hermetically sealed packages with proper electrical conditions and operating junction temperatures of 100 °C or less. For higher temperatures the mean life should be adjusted using the appropriate curve of Figure 7.5-2.
3. This data applies to diodes with or without hermetically sealed packages but with proper electrical conditions and operating temperatures of 100 °C or less. For higher temperatures, the mean life should be adjusted using the appropriate curve of Figure 7.5-2.

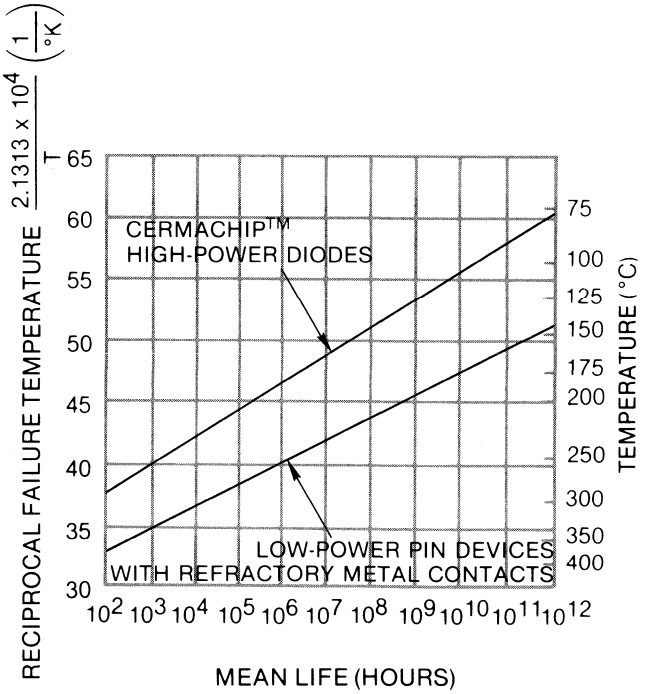


FIGURE 7.5-2 MEAN LIFE VS TEMPERATURE FOR MICROWAVE ASSOCIATES PIN DIODES

bonding and handling procedures for chip and hybrid chip diodes

bonding and handling procedures for chip and hybrid chip diodes

8.1 DISCUSSION

Chip diode devices for use in integrated circuit and hybrid integrated circuits have proliferated in the last few years. The circuit designer today is faced with a multiplicity of alternatives in the selection of diodes and packaging with each choice involving trade-offs of particular advantages and disadvantages. The obvious advantages in the use of chip diodes in hybrid integrated circuit applications are their very small size and potentially lower cost. Small size and simplicity of structure give the benefit of minimal parasitics, but as the size of the diode becomes smaller, handling and production problems increase. We hope that by outlining our own conclusions herein, we may help the designer to overcome some of the difficulties met when using chips in MIC applications.

Microwave Associates manufactures a large selection of chip and packaged diodes for hybrid integrated circuits. See Figure 8.7-1 for a complete listing of Microwave Associates' chip diode configurations. Obviously not all diode types are available in all the configurations. Characteristics such as breakdown voltage or capacitance may limit the size of the chip or its form.

8.1.1 SILICON CHIPS

Hard glass hermetic CERMACHIP™ PIN diodes
Oxide passivated PIN diodes
Beam lead PIN diodes
Snap multiplier diodes
Silicon tuning varactors
MNS chip capacitors
Silicon Schottky diodes
Beam lead silicon Schottky diodes
Low noise RF transistor chips

8.1.2 GALLIUM ARSENIDE CHIP DEVICES

Plated heat sink Gunn diodes
Gunn diode chips
GaAs tuning varactor chips
GaAs parametric amplifier chips
GaAs multiplier chips
GaAs Schottky diode chips
GaAs Hyperabrupt tuning varactor chips
LHL IMPATT diode chips

8.1.3 MICROSTRIP PACKAGES AND CHIP CARRIER

Chip diodes usually require specialized equipment for die attachment to the circuit and for wire or strap bonding to the top of the chip. These operations require a clean work environment and special handling equipment such as vacuum pickups, hot gas bonders and/or thermal compression bonding equipment.

Not all MIC circuits require chips. In many cases (especially for conventional stripline circuits), a hybrid circuit package or carrier will give satisfactory results and can be handled much more easily without a large investment in fabrication equipment.

Microwave Associates supplies a broad line of diodes in stripline or carrier packages. Figure 8.7-1 includes a list of all available hybrid packages and carriers. Section 8.7 discusses assembly methods for hybrid packages.

8.2 HANDLING AND ASSEMBLING OF CHIPS INTO CIRCUITS

The problems of handling and assembling chips into packages can best be separated into two separate areas: putting the chip into the circuit (die down), and making top contact to the chip (top bonding). The following sections will discuss these problems.

8.3 CHIP BONDING METHODS

The biggest problem in using chip diodes is the damage incurred when assembling chips into circuits. In general, the value of the integrated circuit far exceeds the cost of the chip itself. When M/A packaged diodes are used, the critical die-attach and top-contact operations are performed by Microwave Associates, and all devices are RF tested after assembly into the packages. When the circuit fabricator performs the die-attach and wire bonding operation on a complex substrate, he runs the risk of losing or damaging a chip during the bonding operation, which can result in the loss of the whole circuit or an expensive rework cycle.

The most common problems that arise when bonding chips to the circuit are: excessive series resistance, especially under forward bias conditions due to improper bonding of the chip to the ground plane; poor reliability due to entrapment of fluxes under the bond; and mechanical failure of the bond under thermal shock or temperature cycling. All three conditions are the result of improper wetting of the die to the ground plane and are usually caused by inadequate cleanliness or inadequate bonding conditions.

8.3.1 THE INFLUENCE OF THE CIRCUIT BOARD ON CHIP BONDING METHODS

Selection of the chip bonding method must take into consideration the characteristics of the circuit board material being used.

bonding and handling procedures for chip and hybrid chip diodes

Stripline teflon-fiberglass circuits should usually be soft soldered. Most eutectic solders melt at too high a temperature (250-300°C) to be used with teflon-fiberglass boards. Conductive epoxys can also be used but the results may not be as reliable. The use of either IMPATT or Gunn diodes on teflon-fiberglass circuits is not recommended, because the major problem in operating these diodes is the removal of heat. It is absolutely essential that eutectic solders or thermal compression bonding be used to bond these devices to achieve the least thermal resistance. Soft solders and conductive epoxys are not acceptable methods for bonding either Gunn or IMPATT diodes.

The use of beam lead diodes with teflon-fiberglass boards is not generally recommended. Because these boards are flexible, they might be bent during or after bonding and might thus break the diode leads.

In many cases conductive epoxys will give good results with little or no complex equipment required. Although the high temperature and long term reliability of this type of bond is not generally as good as eutectic solders, the use of conductive epoxys is an acceptable and simple way to fabricate most circuits.

Soft solders such as the eutectic composition of tin-antimony or lead-tin give excellent reliability and good high temperature characteristics. The use of flux for soldering is not recommended at any time. Instead, a cover gas such as forming gas (80% N_2, 20% H_2 or 95% N_2, 5% H_2) should be used. When applicable, probably the best die-down procedure is an ultrasonic silicon-gold thermal compression bond or a high temperature eutectic solder such as gold-tin eutectic solder (80% Au, 20% Sn), with melting point at approximately 280°C.

Table 8-A summarizes the characteristics of several methods of chip die-down bonding.

8.4 CHIP DIE-DOWN BONDING TECHNIQUES

8.4.1 HOT GAS BONDING OF CHIPS

The hot gas bonder is one of the most convenient ways to bond chips onto a metal ground plane or cir-

TABLE 8-A SELECTION GUIDE FOR DIE DOWN BONDING TECHNIQUES

DIE DOWN METHOD	RESULTANT THERMAL RESISTANCE	TEMP. REQUIRED	HIGH TEMP. CAPA-BILITIES	POWER HANDLING CAPABILITY	EASE OF OPERATION	SPECIAL EQUIP-MENT REQUIRED	POTENTIAL PROBLEMS
Conductive Epoxy	Good with proper technique	Room temp. to 150°C	Good	Low to medium power	easiest to apply	little or none	High series or thermal resistance
Soft solder i.e. Pb-Sn-Ag (90, 5, 5) Pb-Sn (60, 40)	good to very good	 200-280°C 180-200°C	Good	good to very good for low or high power	simple application	heated stage, hot gas bonder or gas curtain and furnace	Flux is usually required with lead solders. Cleaning of flux must be done carefully
Eutectic solder Au-Sn (80, 20) Sn-Sb (97, 3)	Very good	 approx. 300°C approx. 230°C	Good	Very good	Simple application	heated stage or hot gas bonder	Needs clean reducing atmosphere
Gold silicon Eutectic (Thermal Compression Bond)	Very good	approx. 380°C	Good	Very good	Most difficult	Ultrasonic bonder with heated stage and tip preferable	Cleanliness, proper bonding conditons

bonding and handling procedures for chip and hybrid chip diodes

cuit. The circuit should be plated with a metal such as gold that enhances wetting, and it should be thoroughly cleaned. It is usually a good idea to remove all grease and dirt from the circuit parts by boiling them in reagent grade trichloroethylene and drying them with methanol. The cleaned parts should be stored in a dry atmosphere (RH 20-30% maximum). After cleaning they can be stored for a few days.

Either gold-tin eutectic (80% Au, 20% Sn) MP ≈ 280°C or tin-antimony eutectic (97% Sn, 3% Sb) MP ≈ 232°C solder preforms are very satisfactory with chips that have gold metallization. A gold-germanium eutectic solder may be used for higher temperature operation.

The temperature of the heating stage should be set such that the bonding area quickly rises to within 50-75°C of the melting point of the solder preform. The diameter of the preform should be large enough so that the diagonal of the die (for square dice) fits inside the preform as shown in Figure 8.4-1. An approximately 0.001 to 0.002 inch thick preform is recommended, although this thickness is not critical.

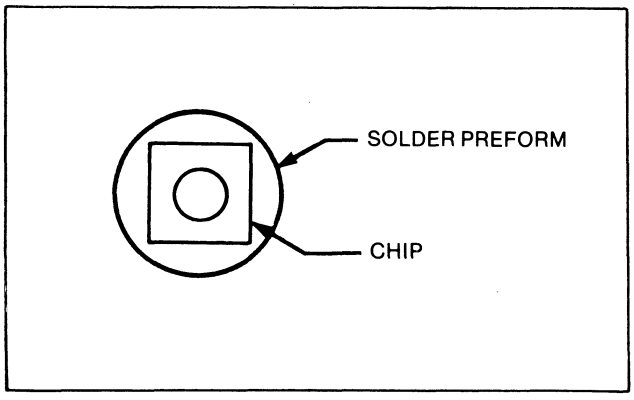


FIGURE 8.4-1 HOT GAS BONDING WITH SOLDER PREFORM

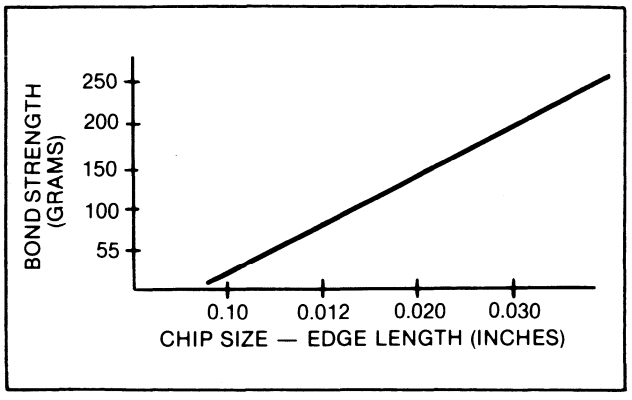


FIGURE 8.4-2 APPROX. MINIMUM BOND SHEAR STRENGTH

We find that 80% N_2, 20% H_2 forming gas is effective as the hot gas jet. The gas temperature at the tip should be approximately 100°C above the solder melting point. The solder should melt in a few seconds after starting the bonding step.

It is a good practice to observe the wetting of the die through a microscope. (A 5-15X microscope will provide enough magnification.) The solder should flow evenly with a smooth shiny surface with no miniscus at the edge. It should wet at least 90 — 95% of the area around the chip. The melted solder should be thin (approximately .001 inch maximum).

A good bond can be tested with a bond strength test. If the bonding is well done, the chip should break at the silicon. Minimum shear strengths for good bonds are shown in Figure 8.4-2. Weak bonds are usually caused by insufficient cleanliness, oxidation of the solder or inadequate heating.

8.4.2 FURNACE SOLDERING OF DICE

A moving belt furnace is also an excellent method to solder chips. A belt furnace with an 80-20 forming gas atmosphere and nitrogen curtains on the ends of the furnace is recommended.

All parts should be clean and free of oil and grease.

The temperature and speed of the belt should be adjusted so that the parts reach approximately 25 — 50°C over the melting point of the solder for a period of 2 — 5 minutes. Adequate tooling and furnace temperature are usually necessary to obtain good alignment. "Clean" gases are also very important. The criteria for acceptable soldered die is shown in Figure 8.4-3.

bonding and handling procedures for chip and hybrid chip diodes

8.4.3 ULTRASONIC THERMAL COMPRESSION BONDING OF DICE

In a small circuit, ultrasonic bonding gives very reliable and strong bonds. The die should be free of oxide and have no metallization. The bonding surface should have approximately 2.5 micrometers of a soft gold, preferably from a high cyanide gold bath.

The stage of the bonder should be set at approximately 200 — 250°C and the bond pressure approximately 400 grams/mm^2.

i.e. approx. 25 gms for 0.010 X 0.010 inch die
approx. 100 gms for 0.020 X 0.020 inch die
approx. 230 gms for 0.030 X 0.030 inch die

These values can vary rather widely and some experimentation may be necessary to find the best results.

The criteria for a good thermal compression bond should be the same as for a soldered joint.

8.4.4 DIE BONDING WITH CONDUCTIVE EPOXYS

Although some military and space systems do not allow the use of conductive epoxies, very satisfactory die-down bonds may be obtained using these epoxys. The following precautions should be observed to obtain consistently strong bonds:

1) **CLEANLINESS** — Everything should be clean and degreased. It is a good idea to clean the circuit in

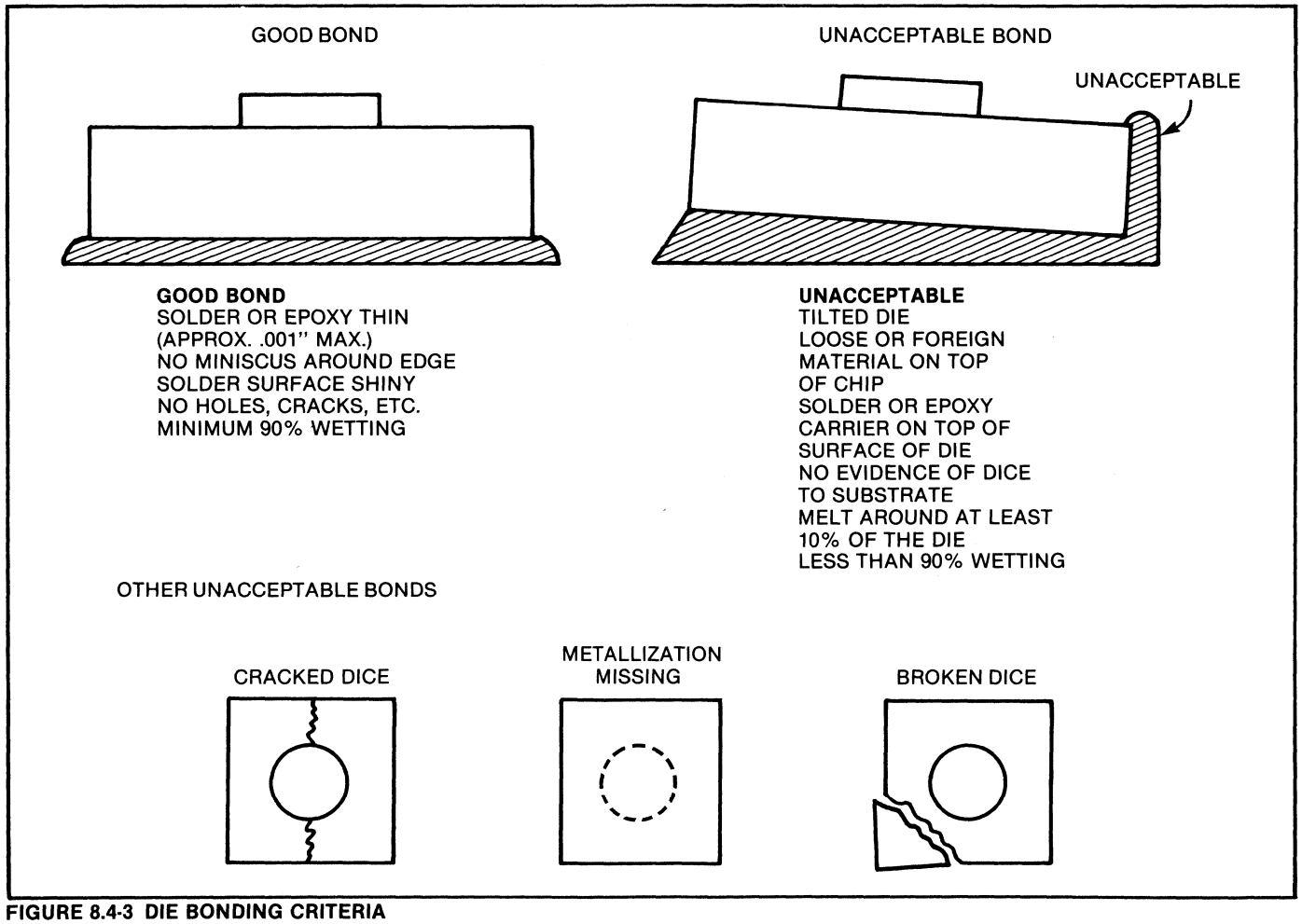


FIGURE 8.4-3 DIE BONDING CRITERIA

bonding and handling procedures for chip and hybrid chip diodes

an alkaline solution to remove any traces of plating solutions and then degrease the circuit.

2) **SHELF LIFE** — The conductive epoxy must be within the warranteed shelf and/or pot life. It is advisable to use one-half the given pot life because manufacturers tend to be optimistic on pot life estimates. Thus, if the pot life is stated to be 2 days, it is much safer to use new epoxy every day.

3) **CURING** — The epoxy must be cured in air or in an oxidizing atmosphere. The reaction requires oxygen. The epoxy oven should be clean (not used for other functions), and should have a good air flow to carry off any carrier fumes. The epoxy will not cure well if there are other solvent fumes in the atmosphere.

4) **CARRIER FLUID** — The carrier fluid must not be allowed to flow on the top of the chip. Not only will it make the chip almost unbondable, but will also be almost impossible to detect under a normal bonding microscope. If a vacuum tip is used to put the chip in place, remove the vacuum when the chip is 10 — 30 mils from the epoxy. Static charge will hold the chip to the tip. If the vacuum tip touches the epoxy it will become coated with the epoxy carrier fluid and will then coat the next chip with the carrier material. This same problem may occur with the use of tweezers. They should be cleaned before picking up another chip (if they touch the epoxy).

5) **RELIABILITY PROBLEMS** — Silver conductive epoxys should not be used where they will come into contact with lead-tin solders or high tin solders. There can be an anodic reaction which may cause failure of the bond.

6) **BOND STRENGTH** — The shear-bond strength of a good epoxy joint can approach that of solder, 50 — 100 kgms/cm^2. The thickness of the conductive epoxy should be kept as thin as 0.001" or less.

   The shear-bond strength should be about:

   40-60 gms for 0.010 x 0.010 inch chip
   150-250 gms for 0.020 x 0.020 inch chip
   350-500 gms for 0.030 x 0.030 inch chip
   See Figure 8.4-2 for minimum bond strength.

   In general, the epoxy will shear before the chip breaks. Weak bonds are usually caused by the use of old epoxy, bonds that are too thick, or lack of cleanliness.

7) **THERMAL RESISTANCE** — Although the thermal resistance of silver conductive epoxy bonds is a little higher than that of gold-tin eutectic solder, it is still satisfactory for all but the highest power applications, as long as the epoxy is kept thin.

8) **VISUAL INSPECTION** — Die-down bonds should be checked regularly using a 5 — 15X microscope and should meet the visual criteria shown in Table 8-B.

TABLE 8-B VISUAL INSPECTION FOR GOOD DIE-DOWN BONDS (USING A 5-15X MICROSCOPE)

DIE DOWN SYSTEM	VISUAL (GOOD BOND CRITERIA)	TYPICAL BOND STRENGTH (IN STRESS)	EXTRA R_S FROM[1] DIE DOWN (.020" CHIP)
Conductive epoxy	Flat and maximum epoxy thickness approx. 0.001 inch. 90% minimum wetting	approx. 50-100 kgms/cm^2	less than 0.15 ohms
Soft Solder	Flat - maximum solder thickness 0.001 inch. 90% minimum wetting	approx. 70-100 kgms/cm^2	less than 0.1 ohms
Gold-tin eutectic solder	Flat, maximum solder thickness 0.001 inch. 90% minimum wetting	approx. 100-150 kgms/cm^2	less than 0.1 ohms
Thermal compression bond	Flat — 90% minimum wetting	approx. 1100 kgms/cm^2	less than 0.1 ohms

1. This is the approximate extra RF series resistance from an ideal lossless bond of a .020" X .020" chip.

bonding and handling procedures for chip and hybrid chip diodes

8.5 TOP BONDING TO THE CHIP

Most chips can be bonded with a wedge bonder. The size and shape of the top contact will depend on the size of the bonding pads and the parasitic inductance or capacitance requirement of the circuit.

A gold strap is most effective for most applications.

Critical criteria in this procedure are the cleanliness, bonding tip shape, tip pressure and stage temperature.

8.5.1 TOP CONTACTING METHODS

The usual criteria for choosing a specific top bonding technique are the size of the top contact of the chip, the type of chip, the sensitivity of the chip to temperature and pressure, the type of circuit board and the equipment available. Table 8-C shows some of the suggested top-bonding methods listed by the type of chip and circuit application. Usually the simplest contact are a gold strap .001 X .005 inch or a 0.0007 to .001 inch diameter wedge bonded gold wire.The inductance of a 1 mil diameter wire will be approximately 0.5 nH for a 0.20 inch long lead. This inductance can be reduced considerably by using multiple contact wires, or by using straps (a technique which also increases reliability).

8.5.2 SELECTION OF BONDING EQUIPMENT, TOOLS AND TIPS

The choice of bonding equipment and tools depends greatly on the type of circuit and chips to be used. Most bonding equipment manufacturers have useful literature available. A very good book on bonding is the **Semiconductor Bonding Handbook** by R. Ellett, of Small Precision Tools, 28 Paul Drive, San Rafael, California 94903.

8.5.3 WIRE BONDING

It is very difficult to give definite parameter values of force, pressure, time and temperature for an optimum bonding schedule. Different wire or strap sizes, bonding surfaces or semiconductor die characteristics require different bonding conditions. In general, the bonding parameters should be adjusted

TABLE 8-C METHODS FOR TOP-BONDING DIODE CHIPS

TYPE OF CHIP	TYPE OF CIRCUIT BOARD	
	CERAMIC	TEFLON FIBERGLASS METAL GROUND
Planar chip with gold metal on anode	Wedge bond 0.002 diameter gold wire or 0.001 X .005 strap. Bonding tool must be smaller than anode pad.	
Beam lead	Ultrasonic bond. Bonding tip size 0.002 maximum. Special tools are available for beam leads.	NOT RECOMMENDED
Schottky diodes with Planar contacts.	Wedge bond 0.0007 diameter gold wire. Bonding tip size 0.001 maximum.	
Hermetic CERMACHIPS™	Wedge bond. 0.001 X 0.005 strap is best Bonding tip size 0.005 maximum.	Wedge bond, or Parallel gap or weld strap
Planar chips with very small anode pads (less than 0.002).	Wedge bond 0.0007 to 0.001 diameter gold wire. Bonding tool size 0.001 maximum.	
Ministrip package	Wedge bond 0.0007 to 0.001 diameter gold wire. Bonding tool size 0.001 maximum.	
Stripline package	Solder or weld leads	
Chip carrier	Wedge bond leads	
Mesa diodes (small)	Wedge bond. Use 5 mil strap, if possible. Bonding tool tip size 0.001 to 0.002.	

bonding and handling procedures for chip and hybrid chip diodes

to maximize reproduceability at a high bond pull strength.

Most problems are caused by improper bonding machine and tool settings as well as improper maintenance and cleanliness. It is important to control the movement of the part being bonded, alignment of tools and work, tool height, angle and tool condition.

In general, the die will crack or "crater" if too hard a wire or excessive pressure is used. Too small a pressure results in small, weak bonds.

A good wire bond should be stronger than the wire and should also be 2 to 3 times the wire diameter as shown in the wire bond of Figure 8.5-1.

Figure 8.5-2 shows scanning electron beam microscope (SEM) photographs of another type of wire bond, the ball bond. As with all top bonds to planar die, the wire (or strap) should break during a pull test before the bond breaks.

When wire bonding, the deformed width of the wire should be about 1.3 to 1.8 times the wire thickness as shown in the through wire bond of Figure 8.5-3.

If the deformed width is too small, the bond will tend to lift off. If it is too large, (greater than about 1.8 times the wire diameter) the wire tends to weaken and break.

Figure 8.5-4 is a curve of the pull strength vs deformed width of ultrasonic bonded wire (by R. Ellett of Small Precision Tool, Inc.).

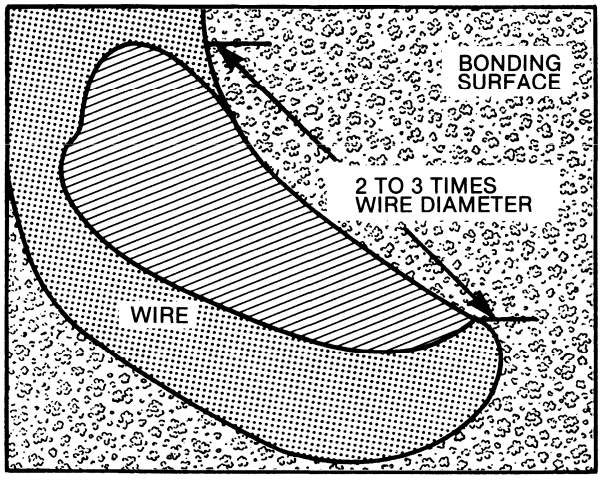


FIGURE 8.5-1 TYPICAL STRONG WIRE BOND

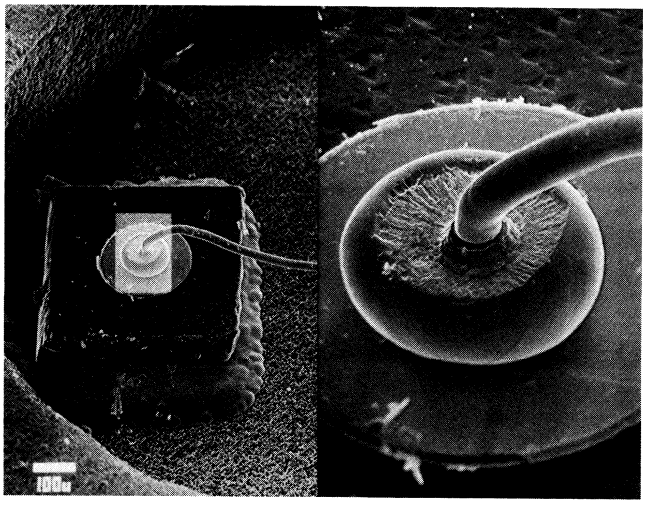


FIGURE 8.5-2 SCANNING ELECTRON BEAM PHOTO OF A GOOD STRAP BOND

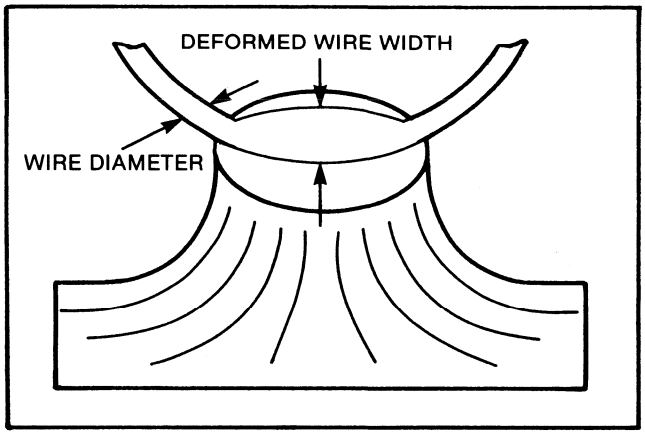


FIGURE 8.5-3 APPROPRIATE WIRE BOND DEFORMATION FOR MAXIMUM STRENGTH

bonding and handling procedures for chip and hybrid chip diodes

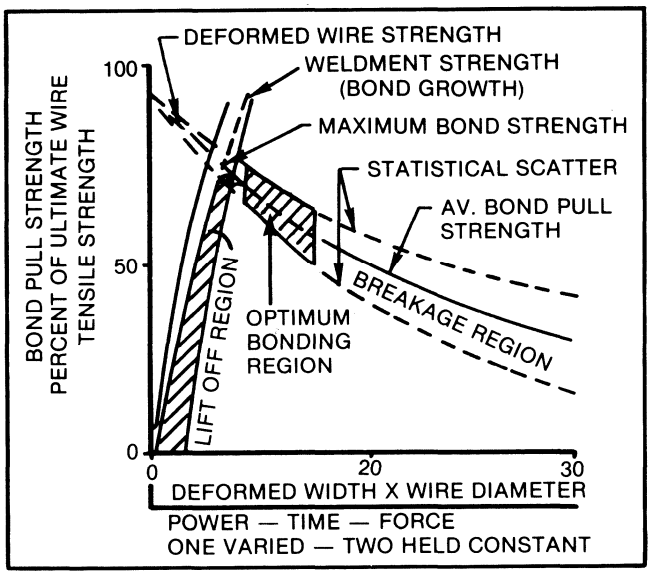


FIGURE 8.5-4 PULL STRENGTH VS DEFORMATION FOR A WIREBOND

8.5.4 STRAP BONDING

When bonding a strap, the bond should not deform the strap by more than 50%. The tool and conditions should be selected to provide a bond that has at least the same cross sectional area as the strap itself. For example, a 0.5 mil X 5 mil strap should have a bond cross section of 2.5 mils sq. or greater. Figure 8.5-5 shows a typical strong

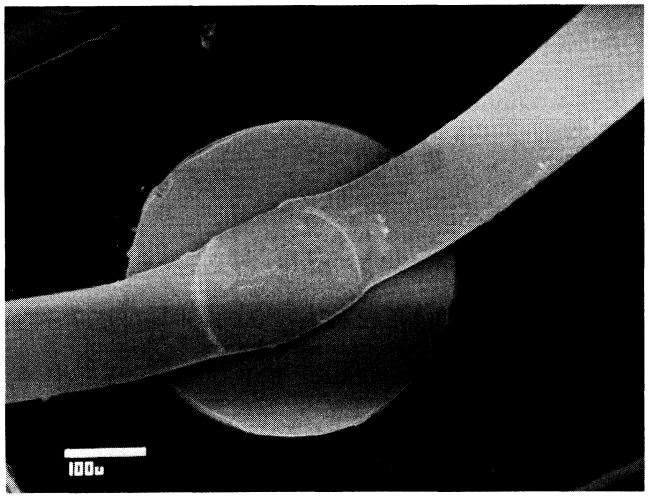


FIGURE 8.5-5 SINGLE STRAP BOND

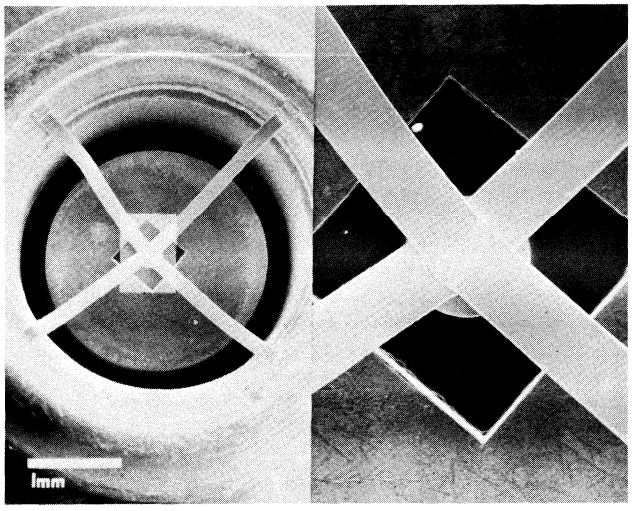


FIGURE 8.5-6 CROSS STRAP BONDING IN A PACKAGED DEVICE

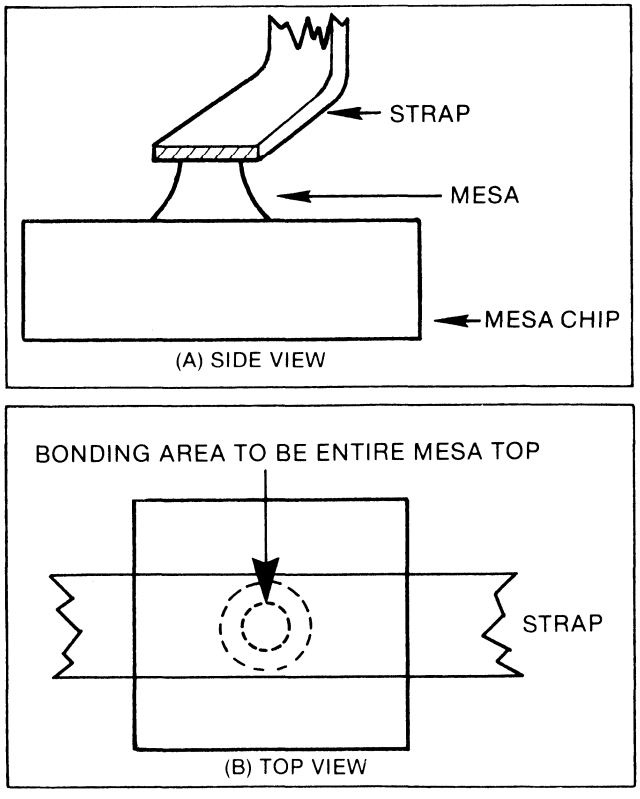


FIGURE 8.5-7 MESA BONDING

bonding and handling procedures for chip and hybrid chip diodes

single strap bond to a large mesa. Cross strapping is used for low parasitic inductance as shown in the SEM photograph of Figure 8.5-6. Very careful heat and pressure control must be exercised in order to form a strong, damage free cross strap bond.

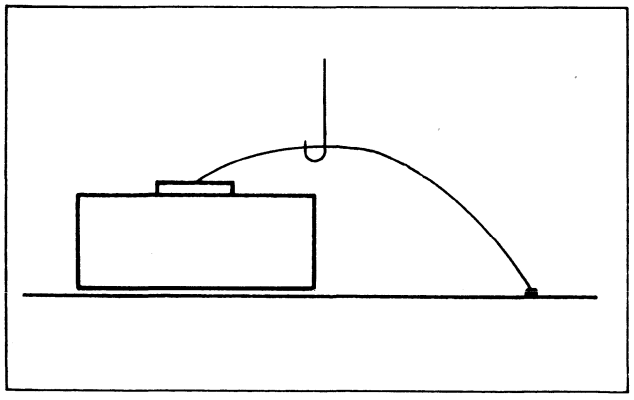
8.5.5 BONDING TO SMALL MESAS

When bonding to a small mesa type diode, we always suggest using a strap. The strap in many cases may or will be larger than the top of the mesa (the larger the cross sectional area of the strap, the lower the parasitic inductance.) In this case it is advisable to bond all or as much of the entire top of the mesa as possible as shown in Figure 8.5-7.

8.5.6 GOOD BONDING CRITERIA

When testing a mesa diode, if the bond is good, the mesa will usually break off before the bond or strap breaks. For all other bonds, the bond should be as strong as the wire or strap when tested by pulling, as shown in Figure 8.5-8. Improper top bonding usually results in one of the following problems:

a) Cracking or stressing the die through excessive pressure.
b) Weak bonds from inadequate cleanliness or improper bonding conditions.
c) Excessive parasitic capacitance from overlapping wires or straps.

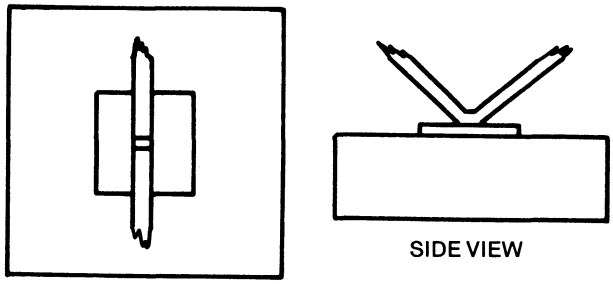


ACCEPTABLE BONDS	BAD BONDS
WIRE OR STRAP DOES NOT SEPARATE WHEN TESTED	WIRE SEPARATES FROM BOND
NO FRACTURES IN BOND	BOND FRACTURES AT WELD
NO SEPARATION OF METALLIZATION	SEPARATION OF METALLIZATION FROM DICE
WIRE BREAKS BEFORE BOND	

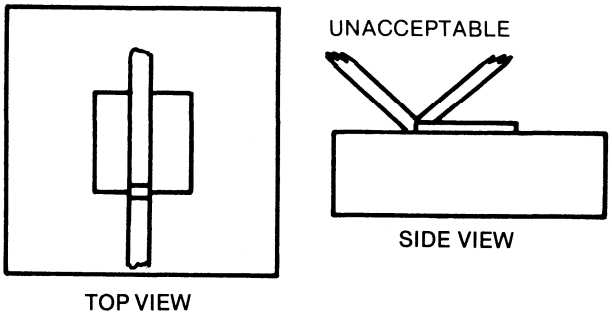
FIGURE 8.5-8 BOND STRENGTH PULL TEST

It is most important to maintain good quality control procedures in order to insure good bonding. The following figures and tables illustrate criteria for visual inspection and for testing of bond strength.

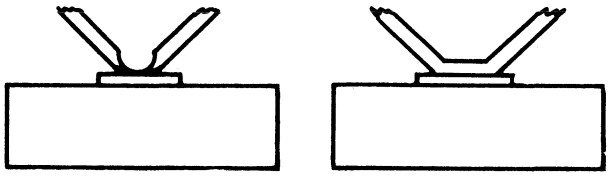
A) GOOD BOND



B) POOR (UNACCEPTABLE) BONDS



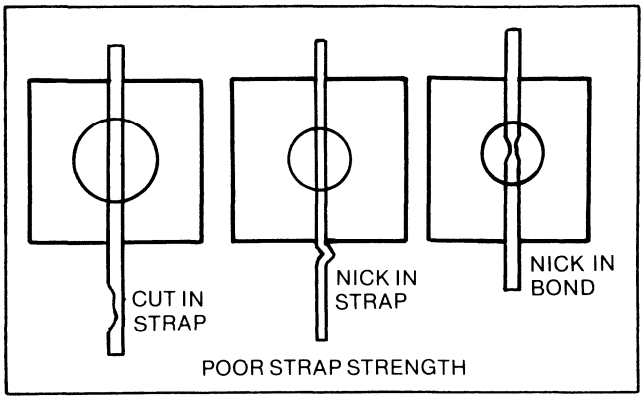
POOR ALIGNMENT



VERY THIN BOND; GOLD PUSHED OUT CAUSED BY A TOO SHARP TIP, TOO MUCH PRESSURE, OR EXCESSIVE HEAT	WEAK BOND — INSUFFICIENT WIRE DEFORMATION

FIGURE 8.5-9 VISUAL BOND INSPECTION CRITERIA FOR GOLD WIRE OR STRAP BONDS

bonding and handling procedures for chip and hybrid chip diodes



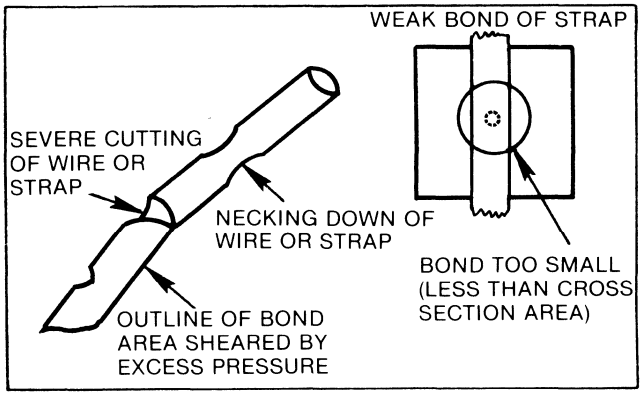


FIGURE 8.5-9 (Continued)

TABLE 8-D BOND STRENGTH CRITERIA (GOLD WIRE OR STRAP)

WIRE-RIBBON SIZE (INCHES)	MINIMUM PULL STRENGTH (GRAMS)
0.0007 WIRE DIAMETER	1.5
0.001 WIRE DIAMETER	3.0
0.002 WIRE DIAMETER	9.0
0.00025 X 0.002 STRAP DIMENSION	1.0
0.00025 X 0.005 STRAP DIMENSION	4.0
0.00025 X 0.010 STRAP DIMENSION	6.5
0.001 X 0.005 STRAP DIMENSION	10
0.001 X 0.010 STRAP DIMENSION	16

8.6 BONDING BEAM-LEAD DIODES

The beam-lead diode is a silicon chip with planar gold leads which extend from the top surface of the chip (approximately 0.010 to 0.030 inch). Beam-lead diodes are generally the smallest-size chips available and may have the smallest parasitics. They are particularly useful as series PIN diodes in broadband switches, because their structure allows for extremely small capacitance. Beam-lead diodes must be handled with care because of their extremely small size . The leads may easily be distorted or broken by the normal pressure of tweezer handling. Most vacuum pencil tips are so large that the vacuum pencil may draw the diode right into the vacuum system.

Beam-lead Schottky diodes, like all other small microwave Schottky diodes, are easily damaged by static electricity or by the current from a small low-impedance ground loop in the circuit. When mounting the diode in the circuit, contact should never be made across the gap; a static discharge from the operator may flow through the diode and destroy it. The circuit should always be grounded before the second lead of the diode is attached.

The two best methods for bonding a beam-lead diode are thermal compression bonding and parallel gap or step welding. For thermal compression bonding, the beam-lead diode is placed down with the leads resting flat on the pad and the bond made by using a heated wedge.

Generally, Microwave Associates has obtained their best results by the parallel gap technique, since it usually results in lower R_S. Current is first passed through the substrate metallization, then through the device lead. Most of the heat is generated at the interface. Extreme care must be taken to see that the step-welder does not discharge through the diode junction, or the diode will be destroyed. The bonding pressure should be the same as for strap bonding (approximately 900 gms/mm^2). The bond criteria given for bonding straps in Section 8.5.6 should be applied to beam-lead diodes as well.

Good equipment for parallel gap welding is available from a number of manufacturers.

When thermal compression bonding the diodes, the bonding tip should be smaller than the thickness of the beam (2 to 3 mils). An ultrasonic bonder usually gives the most satisfactory results. (Especially useful are special bonding tips for ultrasonic bonding of beam leads which allow both leads to be bonded

bonding and handling procedures for chip and hybrid chip diodes

simultaneously.) The major advantage of the parallel gap or step welding technique is that a cold ambient may be used. Heat is only generated in the vicinity of the bond itself. Caution must be taken when making the second bond, for if the diode is placed in tension, the leads may break.

The following precautions will insure better results when bonding beam-leads:

1) To minimize the lead inductance, the wedge, or heated tip should be placed as close as possible to the edge of the chip without touching it. The silicon chip is very easily damaged, and care must be taken that the bonding tip does not contact the chip at any time during the bonding process.

2) Care must also be taken to insure that the bonding tip is perpendicular to the beam during bonding, to prevent a torsional force which will pull the beams apart. This is particularly important when bonding the second lead.

3) The use of beam-leads is not recommended with a soft circuit board such as teflon or fiberglass, since it is very easy to tear or break the beam off by forcing it into the board. If a soft circuit board is used, bonding pressure must be reduced to a minimum to prevent diode breakage.

8.7 BONDING USING MICROSTRIP DIODES AND STRIPLINE PACKAGES

In many cases it is not necessary to use a diode as small in size as the beam-lead diode. A small carrier makes handling much easier. Microwave Associates offers Schottky, PIN and tuning varactor diodes soldered to a small molybdenum tab with either one or two leads. The ministrip package is easily soldered to a circuit. A hot plate, a substrate heater, a belt furnace or a parallel gap welder can be used. (Conductive epoxy may be used for a prototype bonding.) Thermal compression bonding or parallel-gap welding are the processes recommended for attaching the leads. (See Die down procedure.)

Stripline packaged diodes can be used for shunt applications by placing the carrier on the ground plane and attaching the leads to the center conductor. In series application they can be mounted by soldering or welding the leads across a gap. The stripline package, case style 137, is used in a similar way on conventional stripline boards. The leads should be welded for best results .

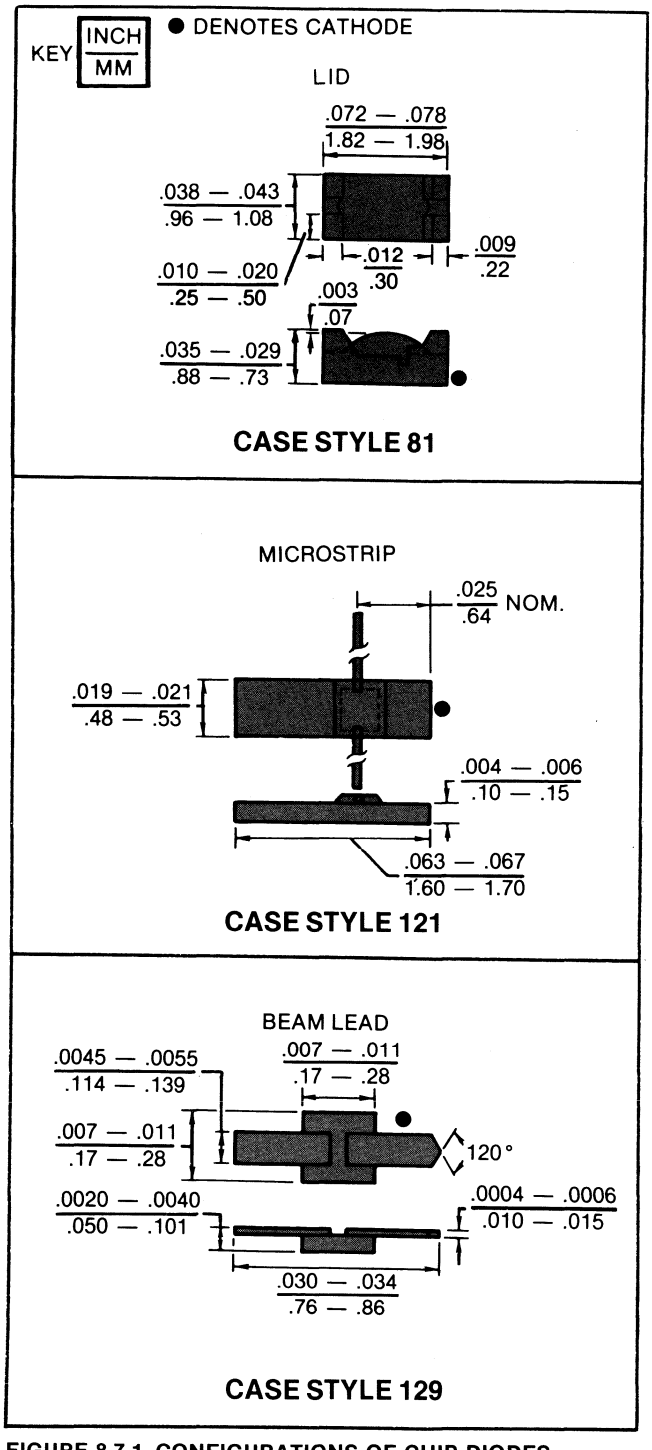
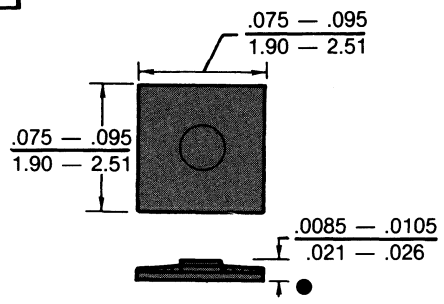


FIGURE 8.7-1 CONFIGURATIONS OF CHIP DIODES (PACKAGE STYLES)

bonding and handling procedures for chip and hybrid chip diodes

KEY INCH / MM ● DENOTES CATHODE

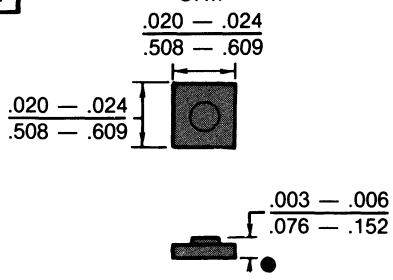
CHIP



CASE STYLE 130

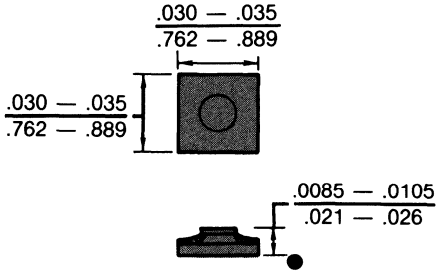
KEY INCH / MM ● DENOTES CATHODE

CHIP



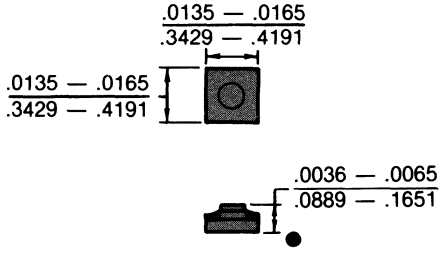
CASE STYLE 133

CHIP



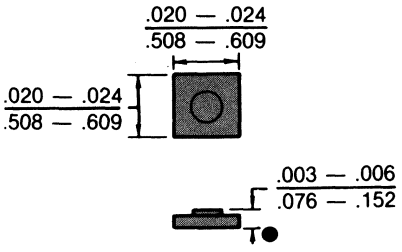
CASE STYLE 131

CHIP



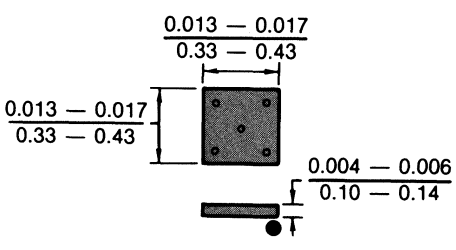
CASE STYLE 134

CHIP



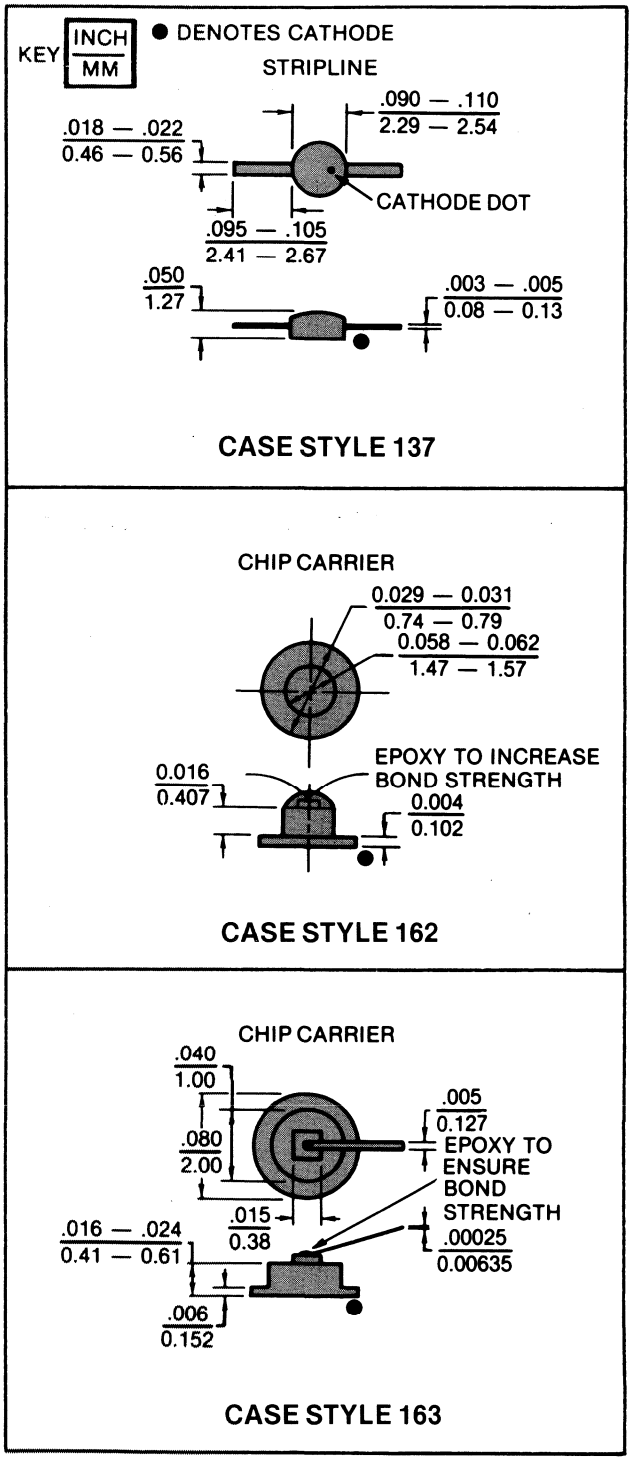
CASE STYLE 132

CHIP



CASE STYLE 135

bonding and handling procedures for chip and hybrid chip diodes



8.7.1 PIN DIODES ON CARRIERS

The microstrip carrier packages are well suited for shunt PIN diode switches and phase shifter circuits. Case styles 162 and 163 are chip carriers. The chip is located in the center of the pedestal, as shown in Figure 8.7-1 to the left. The pedestal allows the electrical and thermal resistance contact to extend up through the board thus reducing inductance. The bottom of the carrier may be attached to the substrate or ground plane with low temperature solder without a large increase in the thermal resistance of the chip to the heat sink. While the pedestal is soldered to the ground plane, the temperature must be kept below 225°C. The wires or straps should be thermal compression bonded or parallel gap welded to the center conductor.

8.7.2 LEADLESS INVERTED DEVICES (LIDS)

Leadless inverted device (LID) diodes are useful in many circuit applications, particularly on fiberglass and teflon circuit boards, because the devices may be attached by soldering rather than bonding. In the LID package (case style 81), the chip is bonded to a ceramic carrier and bonded wires are connected to the pads or "feet". The chip and bonds are then protected from mechanical breakage by filling in the area around the chip with an epoxy resin. The LID package may be bonded to the circuit using simple soldering or flow-soldering techniques.

The best method for attaching a LID package is to pre-tin both the pads of the LID and the pads on the board. The LID can then be soldered using a non-corrosive flux. This method will give the finest results by furnace soldering in a reducing, or non-oxidizing, atmosphere. A small weight can be used to hold the LID tightly against the circuit board. The circuit board, LID and weight or spring should then be brought up to soldering temperature and the solder allowed to flow. The circuit should then be cooled slowly so that a continuous solder fillet will be formed underneath the LID pads. For circuit prototypes or simple circuits, localized heating can be applied from a hot-plate or a hot gas jet. If a soldering iron is used, extreme care must be taken not to overheat the LID. When several LID devices are soldered into a single circuit, a template or solder boat can be used to align all the devices, so they all can be soldered in one operation.

bonding and handling procedures for chip and hybrid chip diodes

In quantity production this can save considerable time as well as improving the reproducibility of the product. The same electrical characteristics are available in LID's as in chip devices. Schottky, PIN, tuning and multiplier diodes may be obtained in the LID package. Figures 8.7-2 and 8.7-3 show how to use LID packages.

Figures 8.7-4 and 8.7-5 summarize the advantages and disadvantages of chips and define hybrid package assembly methods and usage by type of substrate.

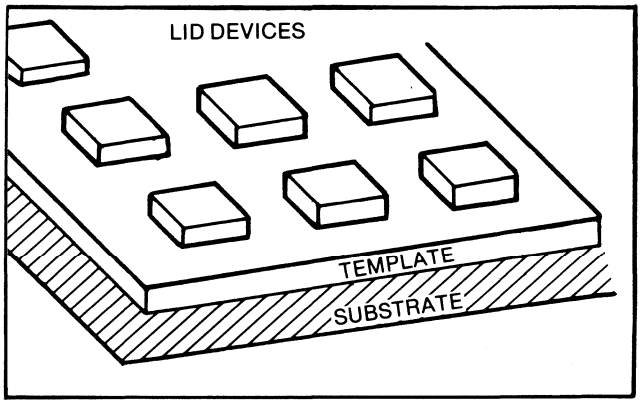


FIGURE 8.7-2 MOUNTED LID DEVICE IN HYBRID INTEGRATED CIRCUIT

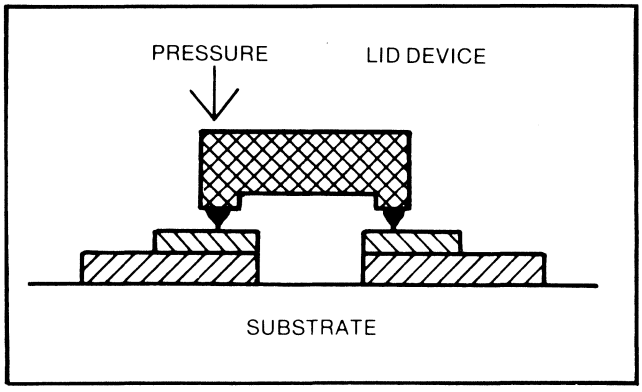


FIGURE 8.7-3 USE OF TEMPLATE FOR MULTIPLE SOLDERING OF LID DEVICES

CHIP CARRIER	BONDING CARRIER TO SUBSTRATE	BONDING RIBBON/WIRE TO TOP CONTACT
Mini Strip	Parallel gap weld Epoxy Soft solder	Wire-thermal comp. bond. Ribbon-thermal comp. bond with ultrasonics.
Top Hat	Press fit Solder (low temp) Base epoxy	as above
LID	Solder (low temp. prewet both parts)	none
Die on round carrier	Solder (low temp.)	Wire-thermal compression bond. Ribbon-thermal comp./with ultrasonic

FIGURE 8.7-5 EXTERNAL CHIP CARRIERS BONDING

bonding and handling procedures for chip and hybrid chip diodes

CHIPS WITH OR WITHOUT LEADS				
TYPE OF BOARD	USABLE DIE DOWN METHODS	BEST METHOD	BOND METHOD	BEST ALL AROUND METHOD
Teflon/Fiberglass	1. Soft solder 2. Conductive epoxy 3. Eutectic solder (usually too hot)	Hot gas bonder Epoxy machine Hot gas bonder	Ultrasonic Ultrasonic	Soft solder (180° max)
Ceramic	1. Eutectic solder 2. Soft solder 3. Conductive epoxy 4. Silicon-gold bond	Hot gas bonder Hot Gas bonder Epoxy machine Ultrasonic bonder	Ultrasonic Ultrasonic	Soft solder or Eutectic solder (280° max.)
Metal Ground Plane	1. Soft solder 2. Conductive epoxy 3. Eutectic solder 4. Silicon gold bond	Hot gas bonder Epoxy machine Hot gas bonder Ultrasonic bonder	Ultrasonic	Soft solder or Eutectic Solder

BEAM-LEADS			MINI STRIP	
TYPE OF BOARD	DIE DOWN METHOD	TOOLS REQUIRED	STRIP DOWN METHOD	TOP CONTACT
Teflon/Fiberglass	Not advised to use		Soft solder (180° max.)	Ultrasonic or parallel step welding wire
Ceramic	Ultrasonic thermal compression wedge Bond with parallel gap weld	Beam lead bonding tool	Soft solder (180° max.)	Ultrasonic bond
Metal Ground Plane	Ultrasonic thermal compression wedge bond parallel gap band	Beam lead bonding tool	Soft solder (180° max.)	Ultrasonic bond

FIGURE 8.7-4 COMPARISON OF BEST DIE DOWN METHOD BY TYPE OF BOARD USED

transistor drivers

transistor drivers

9.1 DISCUSSION

The prime requirement of a driver is to serve as an electronic buffer between command signals and necessary power supplies that bias the PIN diodes. Control signals from the PIN driver may be either unbalanced TTL for short transmission lines, balanced TTL for longer transmission lines or ECL for ultra-high speed switching applications. Drivers may be tailored with extremely rapid driving pulses in order to improve the turn-on or turn-off time of a PIN diode.

Where high RF peak power and reverse bias are involved, the driver must be designed to supply some rectification current during the pulse period in order to prevent thermal runaway and catastrophic device failure. In some drivers, the circuitry is designed to distinguish between PIN and driver failures, and to provide an appropriate signaling indication.

Dual drivers are capable of providing complimentary bias states to more than one PIN diode. For instance, in a SPDT switch, these drivers deliver a forward bias to one diode or diode group while simultaneously providing reverse bias to another diode or diode group.

Transistor drivers for semiconductor control devices may be divided into two basic categories: binary and analog. The binary, or two-state driver circuits, are used for discrete control circuits such as switches, digital phase shifters and duplexers. These drivers, on command, deliver adequate forward current to the PIN diode to drive it into the low impedance or ON state and an opposite command supplies reverse or zero bias voltage that results in a high impedance or OFF state. If adequate voltage and current are supplied to the PIN diode to achieve proper operation of the control circuit over the desired temperature range, no thermal compensation is required.

The analog driver is used when a specific voltage or current profile must be maintained, as in continuous phase shifters or linear attenuators. These drivers may become reasonably complex, since for many applications linearization and temperature compensation are a necessity. Linearization is required when a linear transfer function is desired between the command voltage and the control device attenuation. Thermal compensation may be required if the PIN's R_S varies due to changing environmental temperatures.

9.2 BINARY DRIVERS

The major element of a binary driver is the SPST switch driver. The more complex applications (multi-position switch, transfer switch, etc.) are constructed by matrixing this elemental SPST driver. The SPST switch driver delivers forward current to turn the diode ON and reverse voltage to turn the diode OFF Switching speed and proper bias for RF power are the two most important design considerations for the basic driver.

A typical driver output characteristic is shown in Figure 9.2-1.

The upper half of this waveshape is forward current and the lower half is reverse voltage. The curve shape is deliberate and corresponds to the drive's interactive response to the PIN diode.

The current spike shown at reference point 1 is generated on command from the driver to turn the PIN diode ON. The spike will supply the stored charge required to turn the PIN from its OFF (high resistance) to its ON (low resistance) state. The magnitude of the spike is limited by the forward current limit of the diode (usually in excess of 100 mA). The width of the spike is dictated by the switching speed; high switching speeds will require high, narrow spikes. The area under the current waveform is equal to the stored charge required by the diode. This stored charge is equal to the diode's carrier lifetime multiplied by the steady-state forward current to be applied.

Reference level 2 of Figure 9.2-1 shows the steady-state forward current level. This level should be adequate to keep the diode in the ON state for all operating and environmental conditions. The current

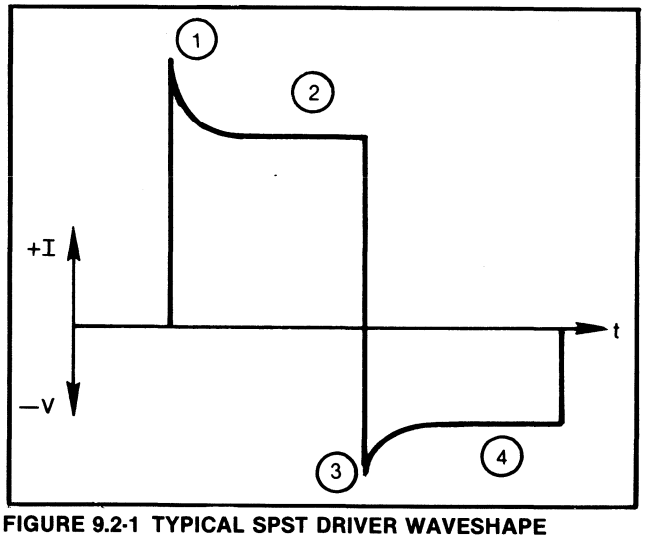


FIGURE 9.2-1 TYPICAL SPST DRIVER WAVESHAPE

required is only that necessary to provide the designed value of R_S. Excessive forward current should be avoided because it will impede switching speed when driving the diode into the OFF state.

The voltage spike of reference point 3 is generated on command to turn the PIN diode OFF. The voltage spike is to remove stored carriers rapidly from the ON state of the diode. This voltage should not exceed the reverse breakdown voltage of the diode. The spike should be narrow for fast switching speeds. Before the diode will switch OFF, its stored charge must be removed. The field created in the diode by the voltage spike sweeps out the remaining carriers from the PIN's I-region and changes the transition capacity of the diode.

Reference level 4 shows the reverse voltage. In high power applications, this level must be adequate to keep the RF power from biasing the diode into the ON state. Excessive reverse voltage should be avoided so that switching speed will not be impeded on return to the ON state.

A block diagram of a typical multiposition (NPNT) transfer or matrix driver is shown in Figure 9.2-2. This driver is simply a stack of SPST drivers controlled from intervening logic.

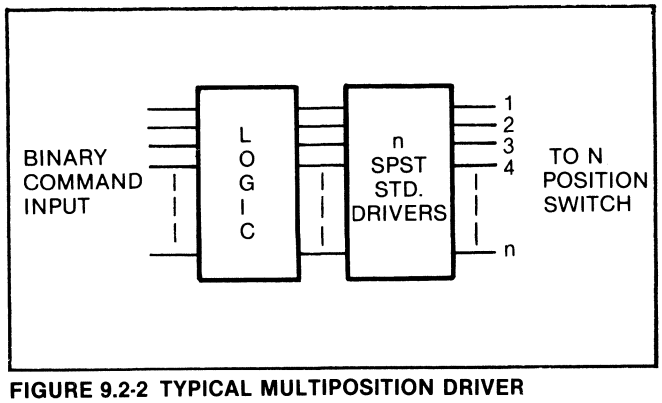


FIGURE 9.2-2 TYPICAL MULTIPOSITION DRIVER

9.3 ANALOG DRIVERS

PIN diodes are commonly used in continuously variable RF attenuators. This is accomplished by changing the diode's forward current. A typical attenuation response at various temperatures is shown in Figure 9.3-1. It should be noted that the curves are not only non-linear but also that there is a drastic performance change with temperature. When this natural behavior is not acceptable, a temperature compensated linearized analog driver can be used to correct these deficiencies.

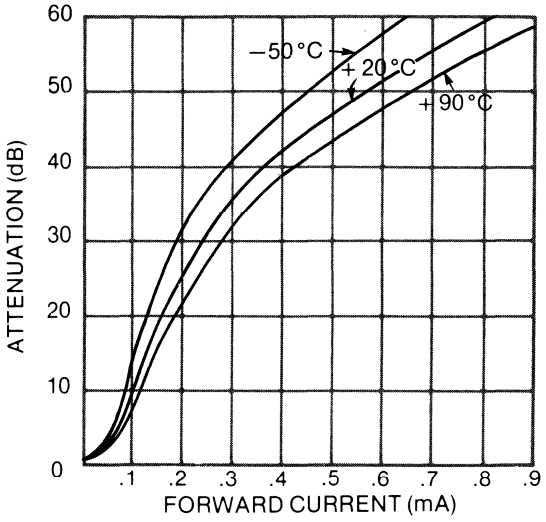


FIGURE 9.3-1 TYPICAL PIN ATTENUATOR PERFORMANCE

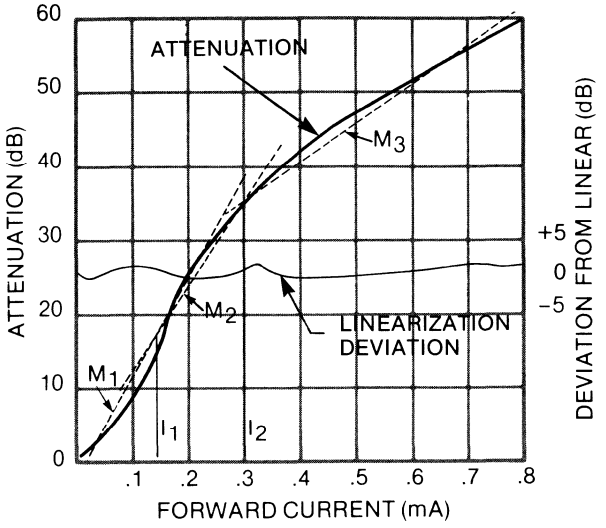


FIGURE 9.3-2 LINEARIZATION CURVE

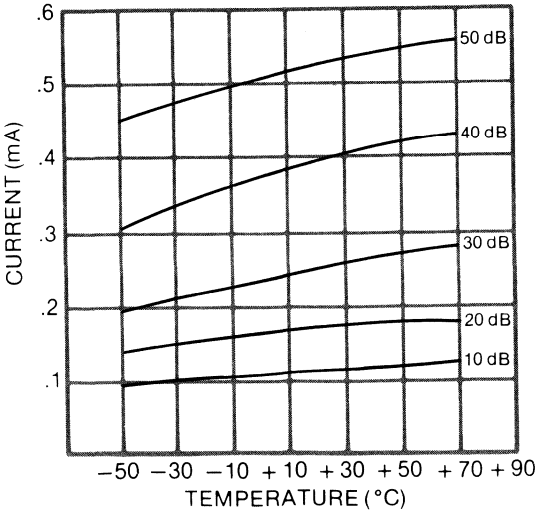


FIGURE 9.3-3 ATTENUATION VS TEMPERATURE

Linearization in an analog driver is achieved by using a variable gain driver. Figure 9.3-2 shows the approach to linearization of a PIN attenuator at room temperature. Note that this curve can be closely simulated by 3 straight lines of slope M_1, M_2 and M_3. Each straight line can represent a driver operating at a different gain, proportional to the slope of the lines. Therefore, the driver is designed to operate at a gain proportional to M_1 from a current level of 0 to I_1. At I_1 (first break point) the driver gain will change to be proportional to M_2 until the current level I_2 is reached. At I_2 (the second break point) the driver gain is again changed to be proportional to M_3. The deviation from these straight line approximations used for the linearization is also shown in Figure 9.3-2.

A typical plot of attenuation as a function of temperature and forward bias is shown in Figure 9.3-3. Because these curves are not linear, temperature compensation is not a simple matter. However, compensation can be accomplished if the curves are considered in two parts; those that extend from room ambient to cold temperatures and those that extend from room ambient to hot temperatures. A temperature bridge is then designed and independently adjusted for each of the two curve families.

For the binary switch driver, switching speed is enhanced by spiking. With the analog driver, spiking can cause overshoot for small attenuation changes. The technique that will permit speed enhancement for an analog driver is known as "proportional spiking". This design technique permits low level spiking for small changes in attenuation and high level spiking for large changes in attenuation.

9.4 SPECIAL DRIVER APPLICATIONS

The increased use of PIN diode devices for **BITE** (Built In Test Equipment) circuits and computer interface circuits has resulted in many special applications for PIN diode drivers. Among them are the closed loop leveling driver, the digitally-controlled analog driver and the Serrodyne.

The function of a closed-loop leveling driver is to provide constant level RF output power in the presence of varying input power. Figure 9.4-1 shows a block diagram of this driver.

The level of output power is sensed through a directional coupler by a back diode detector. The back diode detector generates a frequency and temperature stable voltage whose amplitude variation is a function of RF input power. This voltage is compared to a reference voltage and a correcting current is then transmitted to the PIN attenuator from the differential amplifier. The loop will stabilize when the difference voltage is zero. The result is a frequency and temperature stable power output whose level of stability is a function of the reference voltage stability. A variation of this application derived by periodically varying the reference voltage results in an amplitude modulated RF output signal.

Figure 9.4-2 shows a digitally controlled analog driver for operation from a microprocessor or interface bus.

In this application, the non-linear function is linearized by use of a PROM (Programmable Read Only Memory). The PROM is programmed for the linearizing function. If the computer source software and hardware are extensive, then this linearizing may be accomplished by the computer and the PROM may be eliminated.

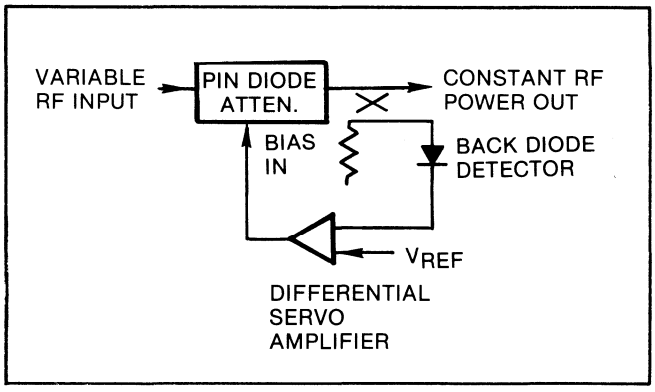


FIGURE 9.4-1 CLOSED-LOOP LEVELING DRIVER

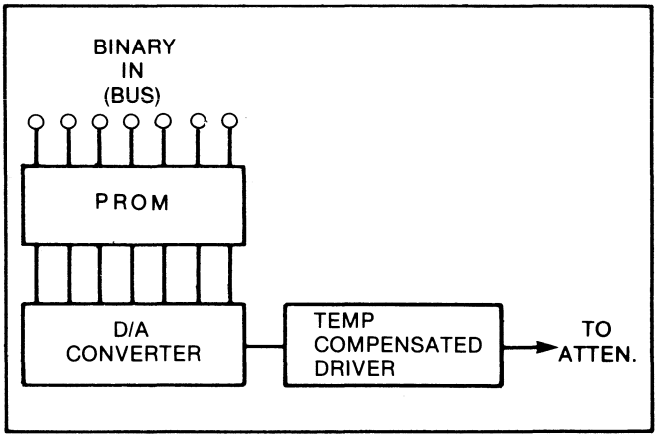


FIGURE 9.4-2 DIGITALLY CONTROLLED ANALOG DRIVER FOR OPERATION FROM MICROPROCESSOR

The Serrodyne circuit, shown in Figure 9.4-3, uses a three bit phase shifter, a square wave logic generator of frequency 8ΔF, two frequency dividers and three binary drivers.

The result is 45° phase steps at frequency 8ΔF, or 360° phase changes at frequency ΔF. This yields a microwave frequency shift generator of ΔF with high carrier suppression as well as high side band suppression (>20 dB).

Driver designs used specifically for matched attenuators are described in Chapter 4.

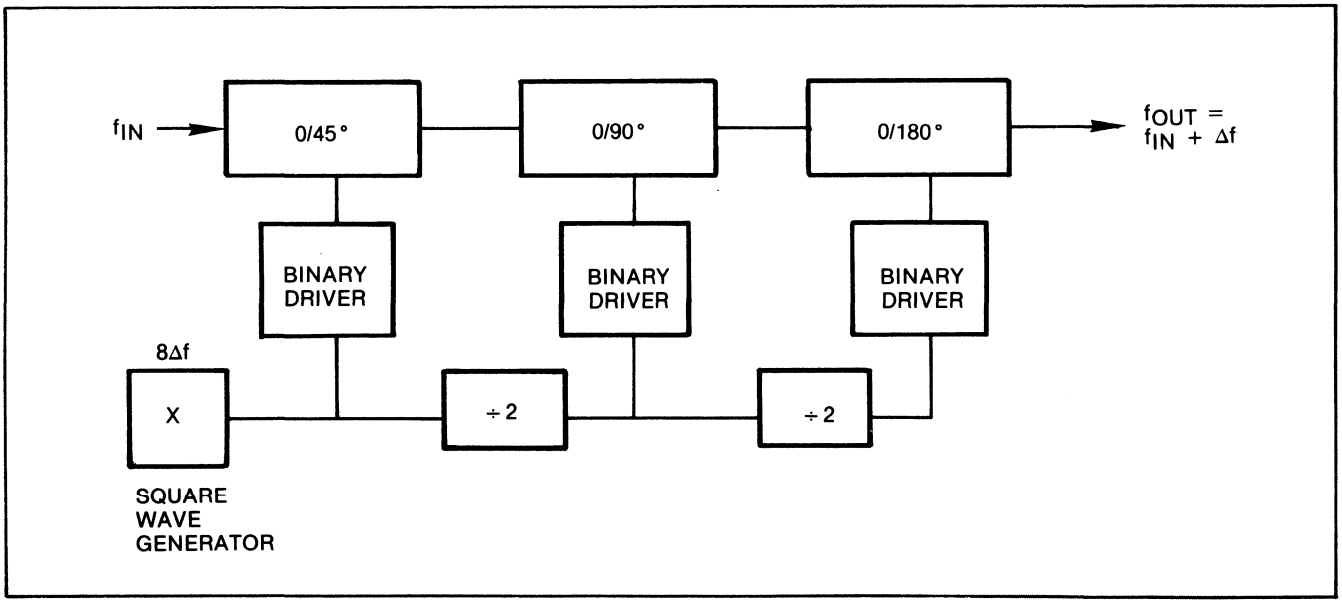


FIGURE 9.4-3 SERRODYNE

PIN specification and switch performance selection guide

PIN specification and switch performance selection guide

10.1 DISCUSSION

In Chapter 2, "The PIN Diode Switch Design Book", the isolation and insertion loss performance of numerous switch types were presented graphically in a generalized form as a function of variable diode parameters. In this chapter, the performance of 16 different Microwave Associates PIN diode types described in the data overview of Chapter 11 (and available from stock) will be described graphically using each in a series of 17 different switch designs, where applicable. In each case the following basic assumptions are made:

1) When more than one PIN is required in a switch, all devices are assumed to be similar.

2) In all cases, it is assumed that no parasitics are encountered.

3) All curves are valid for either PIN diode chips or for packaged PIN diodes if the parasitics C_p (package capacitance) and L_s (lead inductance) are tuned out. (See Chapter 6.)

4) The frequency range under consideration is from 10 MHz to 20 GHz. Plots are presented over the entire frequency range for each switch and PIN type unless electrical performance decays to a point where switching parameters are unreasonable.

5) All transmission lines are assumed to be lossless.

6) The curves apply to a characteristic impedance of 50 ohms except where otherwise specified.

7) The equivalent circuits of Figures 3.1-1 and 3.1-2 apply.

Both isolation and insertion loss performance curves are shown for each of the 16 diodes in the following switch configurations, where applicable:

1) SPST Single-Diode Series Switch
2) SPST Two-Diode Series Switch
3) SPST Three-Diode Series Switch
4) SPST Single-Diode Shunt Switch
5) SPST Two-Diode Shunt Switch
6) SPST Three-Diode Shunt Switch
7) SPST Parallel-Series Switch
8) SPST Two-Diode Shunt-Iterated Switch (λ/4 Spacing)
9) SPST Two-Diode Shunt-Iterated Switch (λ/10 Spacing)
10) SPST Two-Diode Shunt-Iterated Switch (λ/20 Spacing)
11) SPST Three-Diode Shunt-Iterated Switch (λ/4 Spacing)
12) SPST Three-Diode Shunt-Iterated Switch (λ/10 Spacing)
13) SPST Three-Diode Shunt-Iterated Switch (λ/20 Spacing)
14) SPST Two-Diode Series-Iterated Switch (λ/4 Spacing)
15) SPST Two-Diode Series-Iterated Switch (λ/10 Spacing)
16) SPST Two-Diode Series-Iterated Switch (λ/20 Spacing)
17) SPDT Parallel-Series Switch

10.2 SWITCH PERFORMANCE — A SELECTION GUIDE

Table 10-A shows the model numbers and electrical specifications of the Microwave Associates standard PIN product line and will serve as a reference throughout this chapter. As an overview of switching performance, Figure 10.2-1 shows the suggested maximum frequency of usage for each diode or diode array. This determination is based on providing a maximum insertion loss of 1.5 dB and a minimum isolation of 15 dB. The shaded areas on the chart indicate that the maximum frequency listed was limited by excessive insertion loss. The unshaded areas on the chart indicate that the maximum frequency listed was limited by low isolation. Only frequencies up to 20 GHz were analyzed and only series configurations were considered for the beam-lead diodes MA-4P101 and MA-4P102-129. As Figure 10.2-1 shows, when these arbitrary limits were exceeded, series diodes exceeded isolation limits, whereas shunt diodes, in general, exceeded the insertion loss limits.

The switch performance of each Microwave Associates' standard PIN diode and a complete list of its electrical parameters are presented in Section 10.3 through 10.18. All switches are SPST except where stated otherwise.

PIN specification and switch performance selection guide

SWITCH TYPE

CHIP MODEL	SINGLE DIODE SERIES	2 DIODE SERIES	3 DIODE SERIES	SINGLE DIODE SHUNT	2 DIODE SHUNT	3 DIODE SHUNT	2 DIODE PARALLEL-SERIES	3 DIODE 2 PARALLEL-1 SERIES	TEE SWITCH (3 DIODES)	PI SWITCH (3 DIODES)
MA-4P101 (Beam Lead)	14.0	20.0	— —	N/A	N/A	N/A	N/A	N/A	N/A	N/A
MA-4P102-129 (Beam Lead)	5.5	11.5	17.0	N/A	N/A	N/A	N/A	N/A	N/A	N/A
MA-4P102	5.5	11.5	17.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0
MA-4P103	1.9	3.5	5.5	20.0	13.6	9.0	20.0	13.0	20.0	13.0
MA-4P202	5.5	11.5	17.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0
MA-4P203	1.9	3.5	5.5	20.0	13.6	9.0	20.0	13.0	20.0	13.0
MA-4P303	1.9	3.5	5.5	20.0	13.6	9.0	20.0	13.0	20.0	13.0
MA-4P404	1.3	2.6	4.1	20.0	10.0	7.0	20.0	10.0	20.0	10.1
MA-4P504	1.3	2.6	4.1	20.0	10.0	7.0	20.0	10.0	20.0	10.1
MA-4P505	0.80	1.5	2.2	11.5	5.8	4.0	11.8	5.8	11.8	5.8
MA-4P506	0.40	0.82	1.1	5.9	3.0	2.0	6.0	2.9	5.7	2.9
MA-4P604	0.90	1.8	2.8	13.5	7.0	4.5	13.0	6.5	12.0	6.6
MA-4P606	0.45	0.90	1.4	7.0	3.2	2.3	6.8	3.4	6.5	3.4
MA-4P607	0.20	0.40	0.60	3.0	1.6	1.1	3.1	1.5	3.0	1.5
MA-4P608	0.11	0.21	0.35	1.5	0.80	0.55	1.6	0.80	1.6	0.80
MA-4P709	0.08	0.15	0.25	1.2	0.60	0.40	1.2	0.60	1.2	0.60

FIGURE 10.2-1 SUGGESTED MAXIMUM FREQUENCY[1] FOR M/A CHIPS AND LIMITING SWITCH PARAMETER FOR VARIOUS SWITCHING CONFIGURATIONS

NOTE:

1. The maximum frequency of usage (GHz) is based on either of the following arbitrary criteria:
   a) Insertion loss approx. ≤ 1.5 dB
   b) Isolation approx. ≥ 15 dB
   Obviously the relative performance of the various switch types within the above criteria differs drastically. The analysis is restricted to frequencies below 20 GHz for the same diode or diodes.
   Only series configurations were considered in analyzing beam-lead diodes.
   Switches are SPST unless noted otherwise.
   Diode models are listed by order of increasing model number.
   Shaded areas indicate the maximum frequency listed was limited by excessive insertion loss.
   Unshaded areas indicate the maximum frequency listed was limited by low isolation.

PIN specification and switch performance selection guide

SWITCH TYPE (Continued)

CHIP MODEL	2 SHUNT ITERATED DIODES λ/4 APART	2 SHUNT ITERATED DIODES λ/10 APART	2 SHUNT ITERATED DIODES λ/20 APART	3 SHUNT ITERATED DIODES λ/4 APART	3 SHUNT ITERATED DIODES λ/10 APART	3 SHUNT ITERATED DIODES λ/20 APART	2 SERIES ITERATED DIODES λ/4 APART	2 SERIES ITERATED DIODES λ/10 APART	2 SERIES ITERATED DIODES λ/20 APART	SPDT SWITCH PARALLEL-SERIES (4 DIODES)
MA-4P101 (Beam Lead)	N/A	N/A	N/A	N/A	N/A	N/A	20.0	20.0	20.0	N/A
MA-4P102-129 (Beam Lead)	N/A	N/A	N/A	N/A	N/A	N/A	19.0	19.0	17.0	N/A
MA-4P102	20.0	20.0	20.0	20.0	20.0	20.0	19.0	19.0	17.0	20.0
MA-4P103	20.0	20.0	17.0	20.0	20.0	8.6	6.2	6.2	5.9	20.0
MA-4P202	20.0	20.0	20.0	20.0	20.0	20.0	19.0	19.0	17.0	20.0
MA-4P203	20.0	20.0	17.0	20.0	20.0	8.6	6.2	6.2	5.9	20.0
MA-4P303	20.0	20.0	17.0	20.0	20.0	8.6	6.2	6.2	5.9	20.0
MA-4P404	18.0	20.0	13.0	20.0	20.0	6.5	4.8	5.0	4.1	20.0
MA-4P504	18.0	20.0	13.0	20.0	20.0	6.5	4.8	5.0	4.1	20.0
MA-4P505	10.2	20.0	7.0	12.2	17.0	6.6	2.7	2.7	2.30	12.0
MA-4P506	5.1	16.0	3.6	6.3	8.5	3.4	1.4	1.42	1.20	6.0
MA-4P604	12.0	20.0	8.0	14.0	20.0	7.5	3.2	3.2	2.80	12.5
MA-4P606	6.0	17.0	4.2	7.5	10.0	3.8	1.6	1.62	1.40	6.5
MA-4P607	2.7	8.2	1.9	3.4	4.5	1.7	0.71	0.72	0.66	3.0
MA-4P608	1.4	4.2	1.0	1.8	2.4	0.90	0.38	0.40	0.35	1.6
MA-4P709	1.1	3.1	0.75	1.3	1.7	0.70	0.29	0.30	0.26	1.2

PIN specification and switch performance selection guide

TABLE 10-A SPECIFICATIONS FOR STANDARD PINS

MODEL NUMBER	MA-4P101 Beam Lead	MA-4P102 -129 Beam Lead	MA-4P102	MA-4P103	MA-4P202	MA-4P203	MA-4P303	MA-4P404
CASE STYLE	129	129	30	30	30	30	30	30
Minimum V_B[1] (Volts)	40	40	50	30	100	100	200	300
Maximum Cj[2] @ V_R (pF)(Volts)	.02 @ 10	.05 @ 10	.05 @ 10	.15 @ 10	.05 @ 10	.15 @ 10	.15 @ 10	.20 @ 50
Maximum R_S[3] @ I_F (Ohms)(mA)	8 @ 10	6 @ 10	2.5 @ 10	1.5 @ 20	2.0 @ 10	1.5 @ 10	1.5 @ 10	0.6 @ 50
Typical τ_L[4] (μs)	.200	.200	.100	.010	.100	.100	.200	1.0
Typical T_{rr}[5] (μs)	.003	.003	.005	.001	.005	.020	.065	.140
Maximum θ jc (°C/Watt)	600	600	60	40	60	30	30	20

MODEL NUMBER	MA-4P504	MA-4P505	MA-4P506	MA-4P604	MA-4P606	MA-4P607	MA-4P608	MA-4P709
CASE STYLE	30	30	30	30	30	43	43	150
Minimum V_B[1] (Volts)	500	500	500	1000	1000	1000	1000	1500
Maximum Cj[2] @ V_R (pF)(Volts)	.20 @ 100	.35 @ 100	.70 @ 100	.30 @ 100	.60 @ 100	1.3 @ 100	2.5 @ 100	3.3 @ 100
Maximum R_S[3] @ I_F (Ohms)(mA)	0.6 @ 100	4.5 @ 100	0.3 @ 100	1.2 @ 100	0.7 @ 100	0.4 @ 100	.35 @ 100	.35 @ 200
Typical τ_L[4] (μs)	2.0	2.0	3.0	3.0	4.0	5.0	5.0	8.0
Typical T_{rr}[5] (μs)	.350	.350	.350	.700	1.0	1.5	1.5	2
Maximum θ jc (°C/Watt)	20	15	10	20	10	7	5	2

NOTES:

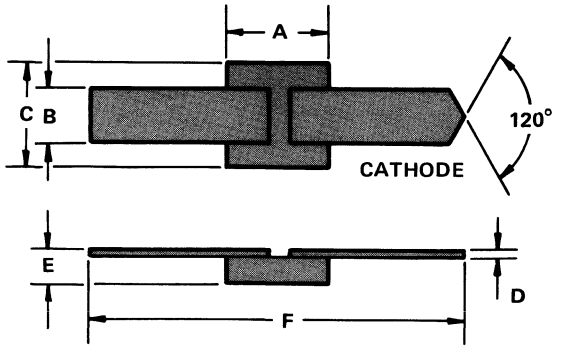
1. Breakdown voltage is measured at -10μA.
2. Capacitance is measured at 1 MHz.
3. Series resistance, R_S, is measured at 500 MHz.
4. Minority carrier lifetime, τ_L, is determined at the 90% recovery point with I_F = 10 mA and I_R = 6 mA.
5. Reverse recovery time, T_{rr}, is determined at the 90% recovery point with I_F = 20 mA and I_R = 200 mA.

PIN specification and switch performance selection guide

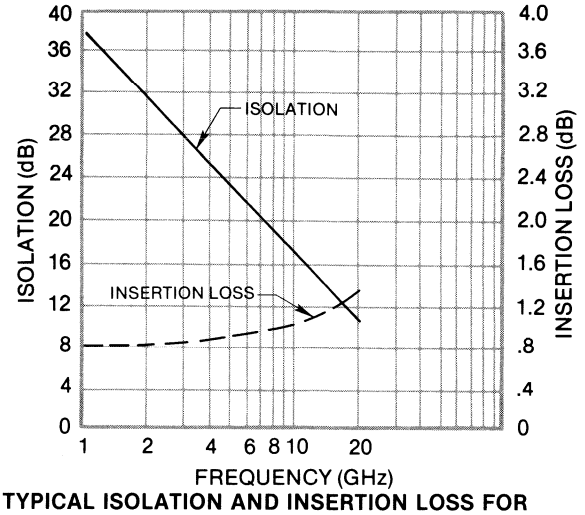
10.3 MA-4P101 (BEAM LEAD) SPECIFICATIONS AND SWITCHING PERFORMANCE

Voltage Breakdown (V_b) = 40 volts (MIN) @ 10μA
Junction Capacitance (C_j) = .02 pF (MAX) @ 10 volts
Series Resistance (R_S) = 8Ω (MAX) @ 10 mA
Carrier Lifetime (τ_L) = .20μs (TYP)
Reverse Recovery Time (T_{rr}) = 3 ns (TYP)
Thermal Resistance (θ_{jc}) = 60°C/W (MAX)
Power Dissipation @ 25°C = 250 mW (MAX)
Standard Case Style = 129

The MA-4P101 is a beam lead PIN diode that features extremely low junction capacitance and minimal parasitics resulting in high isolation over a broad frequency band. This device is designed specifically for either single or multiple diode series switches at frequencies up to 20 GHz in stripline or microstrip environments.



DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.011	0.007	0,28	0,17
B	0.0055	0.0045	0,139	0,114
C	0.011	0.007	0,28	0,17
D	0.0006	0.0004	0,15	0,010
E	0.0040	0.0020	0,101	0,050
F	0.034	0.030	0,86	0,76



TYPICAL ISOLATION AND INSERTION LOSS FOR MA-4P101 USED IN AN UNTUNED STRIPLINE CIRCUIT

PIN specification and switch performance selection guide

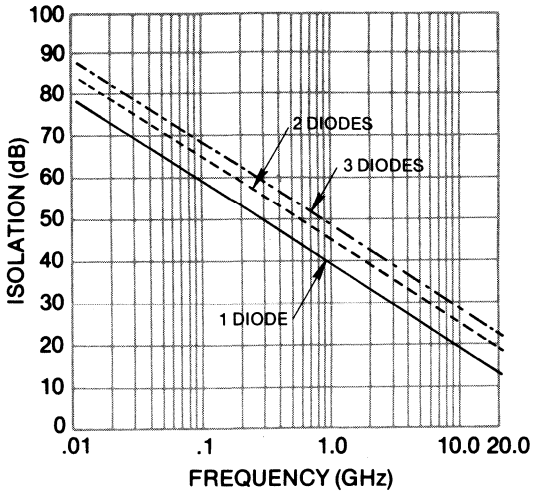


FIGURE 10.3-1 MA-4P101 SERIES DIODES — ISOLATION VS FREQUENCY

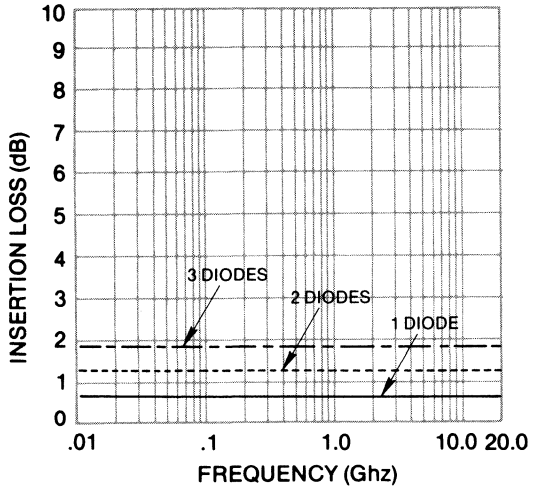


FIGURE 10.3-2 MA-4P101 SERIES DIODES — INSERTION LOSS VS FREQUENCY

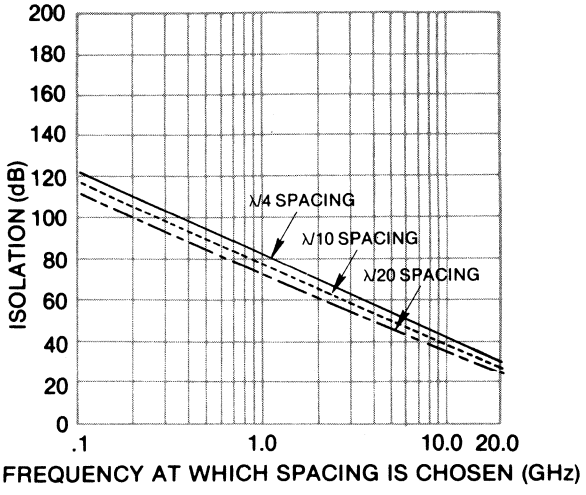


FIGURE 10.3-3 TWO SERIES-ITERATED MA-4P101 SERIES DIODES — λ/4, λ/10, λ/20 APART — ISOLATION VS FREQUENCY

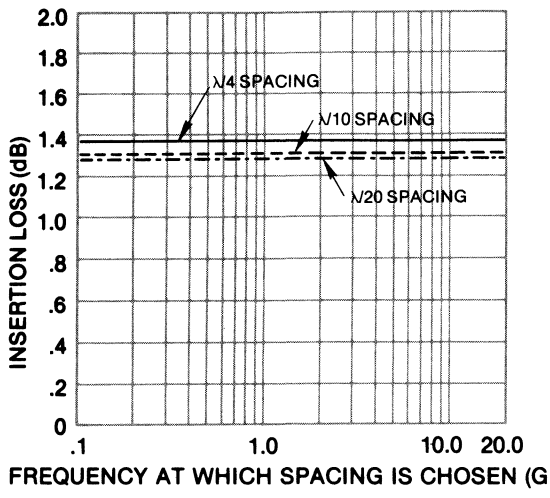


FIGURE 10.3-4 TWO SERIES-ITERATED MA-4P101 DIODES — λ/4, λ/10, AND λ/20 APART — INSERTION LOSS VS FREQUENCY

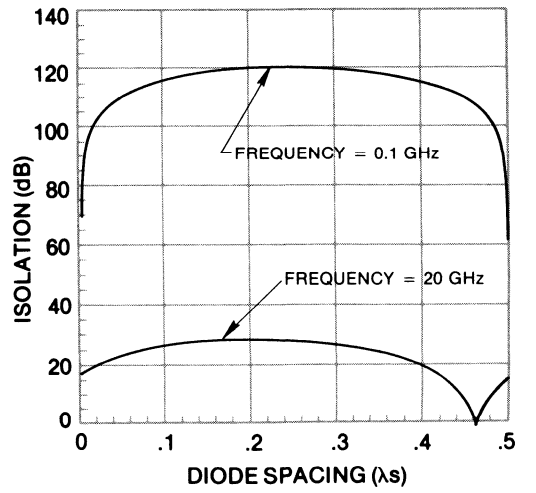


FIGURE 10.3-5 TWO SERIES-ITERATED MA-4P101 DIODES — ISOLATION VS SPACING

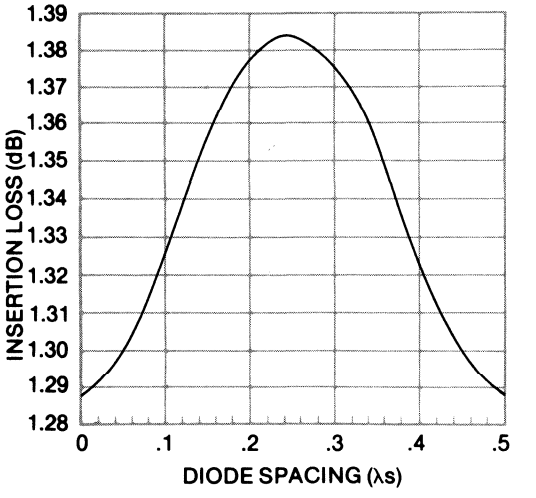


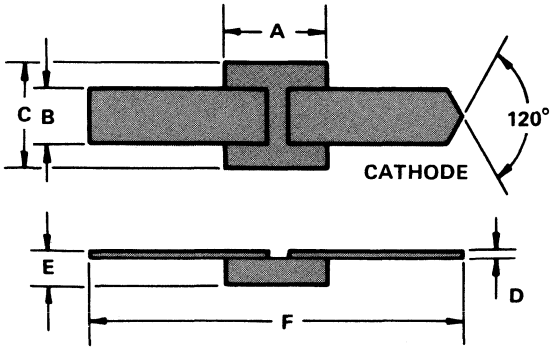
FIGURE 10.3-6 TWO SERIES-ITERATED MA-4P101 DIODES — INSERTION LOSS VS SPACING

PIN specification and switch performance selection guide

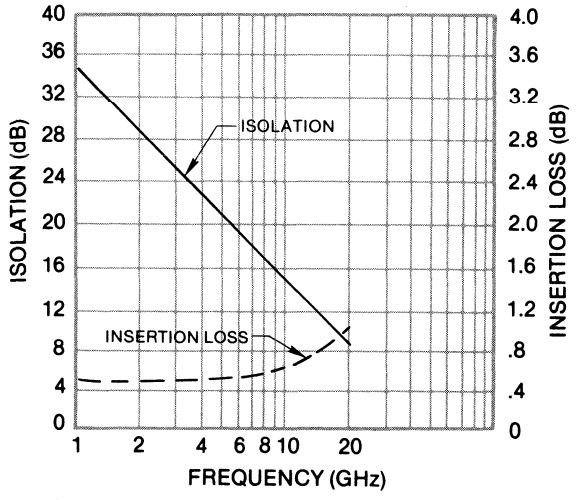
10.4 MA-4P102-129 (BEAM LEAD) SPECIFICATIONS AND SWITCHING PERFORMANCE

Voltage Breakdown (V_b) = 40 volts (MIN) @ 10μA
Junction Capacitance (C_j) = .05 pF (MAX) @ 10 volts
Series Resistance (R_S) = 6Ω (MAX) @ 10 mA
Carrier Lifetime (τ_L) = .20μs (TYP)
Reverse Recovery Time (T_{rr}) = 3 ns (TYP)
Thermal Resistance (θ_{jc}) = 60°C/W (MAX)
Power Dissipation @ 25°C = 250 mW (MAX)
Standard Case Style = 129

The MA-4P102-129 is another member of the M/A beam lead PIN diode family. This device is designed specifically for low insertion loss in either single- or multiple-diode series switching arrays at frequencies up to 20 GHz in stripline or microstrip environments.



DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.011	0.007	0,28	0,17
B	0.0055	0.0045	0,139	0,114
C	0.011	0.007	0,28	0,17
D	0.0006	0.0004	0,15	0,010
E	0.0040	0.0020	0,101	0,050
F	0.034	0.030	0,86	0,76



TYPICAL ISOLATION AND INSERTION LOSS FOR MA-4P102 USED IN AN UNTUNED STRIPLINE CIRCUIT

PIN specification and switch performance selection guide

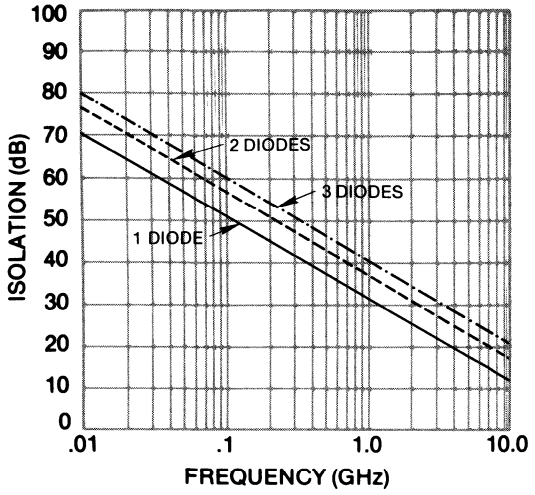


FIGURE 10.4-1 MA-4P102-129 SERIES DIODES — ISOLATION VS FREQUENCY

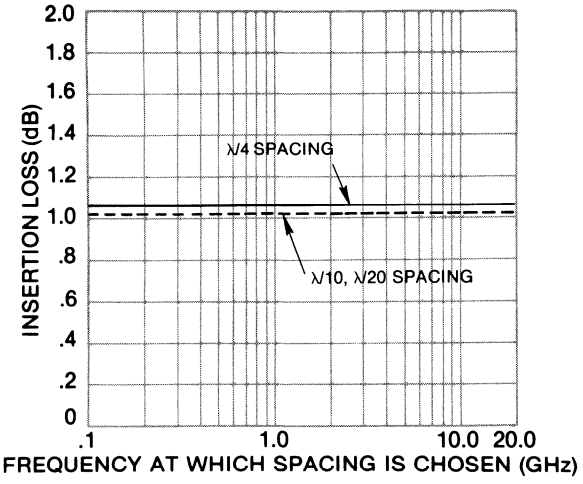


FIGURE 10.4-2 MA-4P102-129 SERIES DIODES — INSERTION LOSS VS FREQUENCY

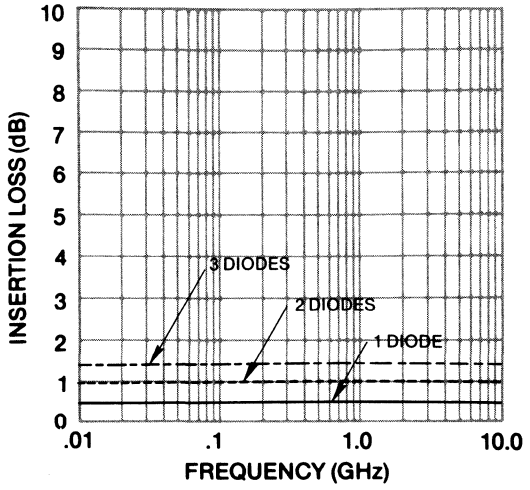


FIGURE 10.4-3 TWO SERIES-ITERATED MA-4P102-129 DIODES — λ/4, λ/10, λ/20 APART ISOLATION VS FREQUENCY

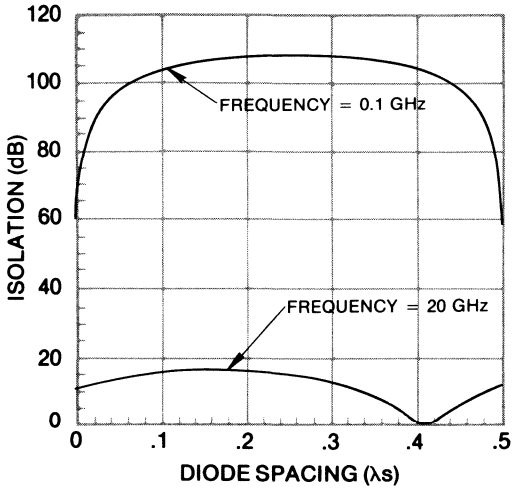


FIGURE 10.4-4 TWO SERIES-ITERATED MA-4P102-129 DIODES λ/4, λ/10, λ/20 APART INSERTION LOSS VS FREQUENCY

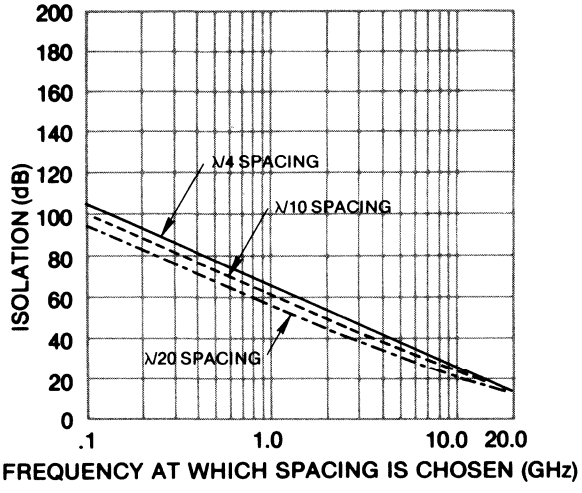


FIGURE 10.4-5 TWO SERIES-ITERATED MA-4P102-129 DIODES — ISOLATION VS SPACING

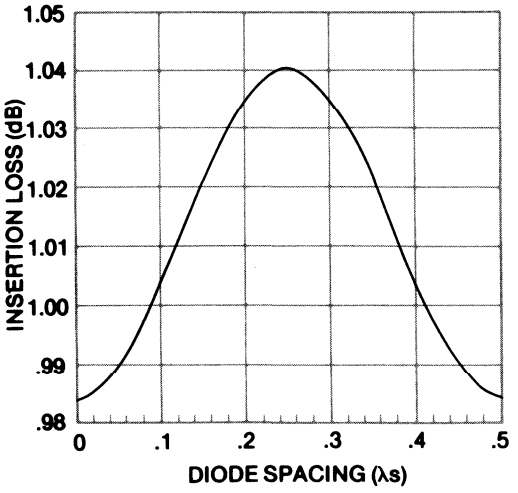


FIGURE 10.4-6 TWO SERIES-ITERATED MA-4P102-129 DIODES — INSERTION LOSS VS SPACING

PIN specification and switch performance selection guide

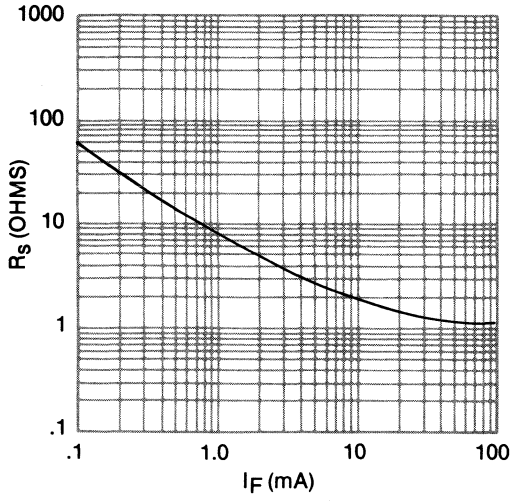
10.5 MA-4P102 SPECIFICATIONS AND SWITCHING PERFORMANCE

Voltage Breakdown (V_b)	=	50 volts (MIN) @ 10μA
Junction Capacitance (C_j)	=	.05 pF (MAX) @ 10 volts
Series Resistance (R_S)	=	2.5Ω (MAX) @ 10 mA
Carrier Lifetime (τ_L)	=	.10μs (TYP)
Reverse Recovery Time (T_{rr})	=	5 ns (TYP)
Thermal Resistance (θ_{jC})	$\approx$	60 °C/W (MAX)
Power Dissipation @ 25 °C	=	2.5W (MAX)
Standard Case Styles[1]	=	30, 54 and 134

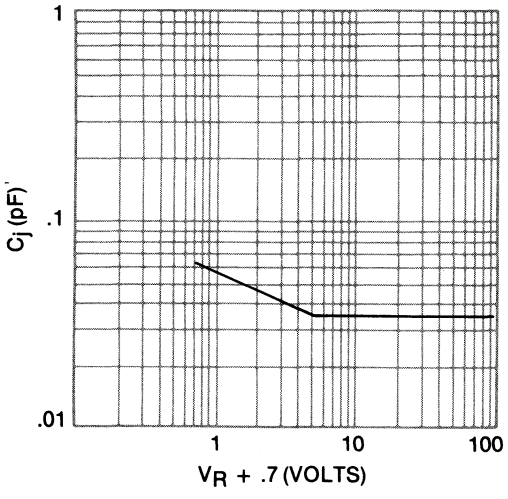
The MA-4P102 PIN diode is specifically designed for low level limiting, ultra-fast switching, (typically 5 ns) and pulse code modulation applications. These devices feature very low capacitance values for high frequency broadband applications.

NOTE:

1. Custom packaging is available upon request.



SERIES RESISTANCE (R_S) VS FORWARD CURRENT (I_F) FOR AN MA-4P102 PIN DIODE



JUNCTION CAPACITANCE (C_j) VS REVERSE VOLTAGE (V_R) FOR AN MA-4P102 PIN DIODE

PIN specification and switch performance selection guide

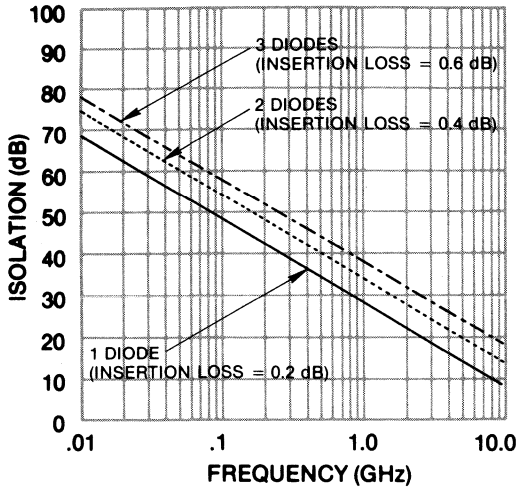


FIGURE 10.5-1 MA-4P102 SERIES DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

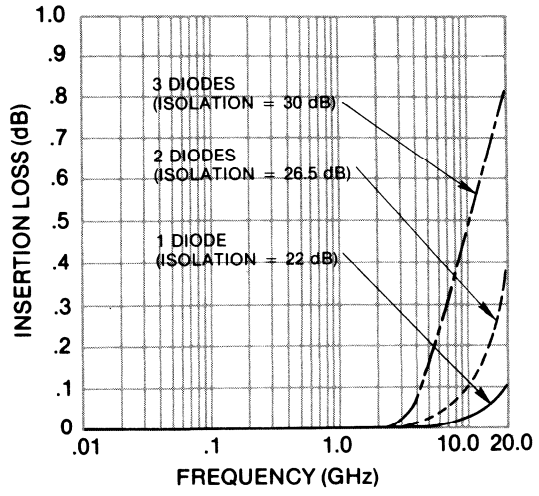


FIGURE 10.5-2 MA-4P102 SHUNT DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

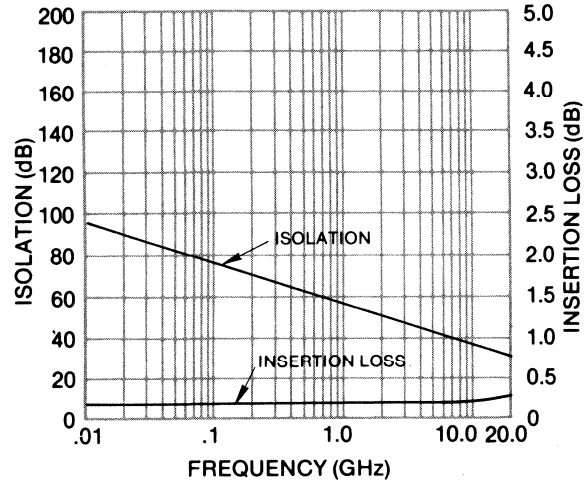


FIGURE 10.5-3 MA-4P102 PARALLEL-SERIES SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

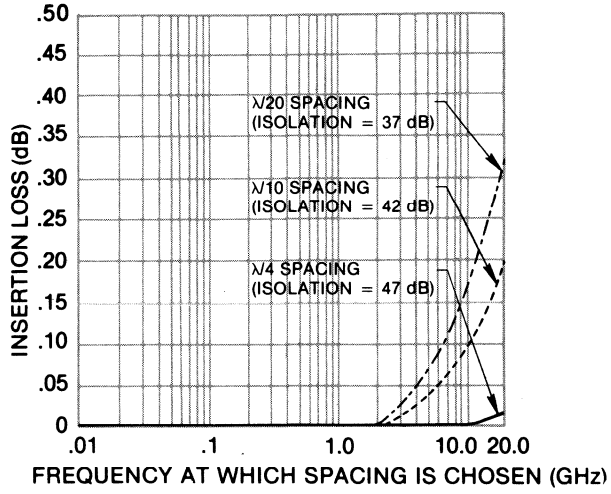


FIGURE 10.5-4 TWO SHUNT-ITERATED MA-4P102 DIODES — λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

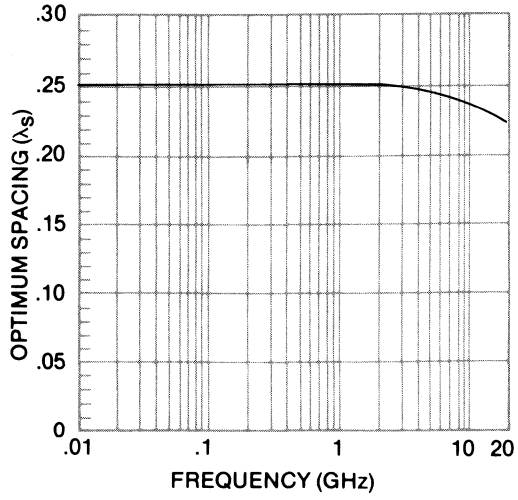


FIGURE 10.5-5 TWO ITERATED MA-4P102 SHUNT DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

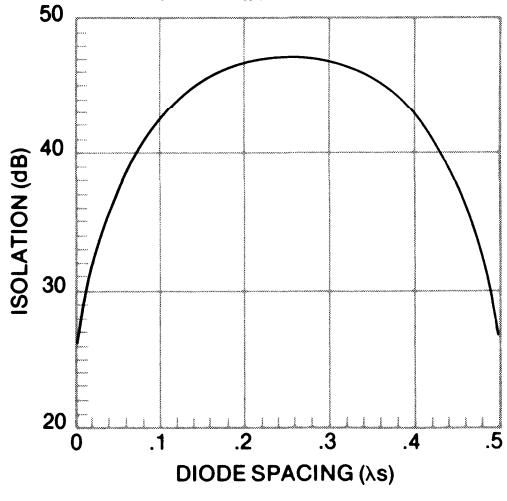


FIGURE 10.5-6 TWO ITERATED MA-4P102 SHUNT DIODES — ISOLATION VS SPACING

PIN specification and switch performance selection guide

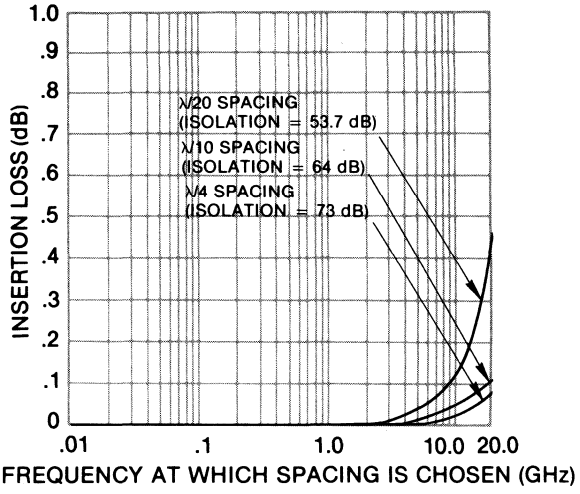


FIGURE 10.5-7 THREE SHUNT-ITERATED MA-4P102 DIODES, λ/4, λ/10 AND λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

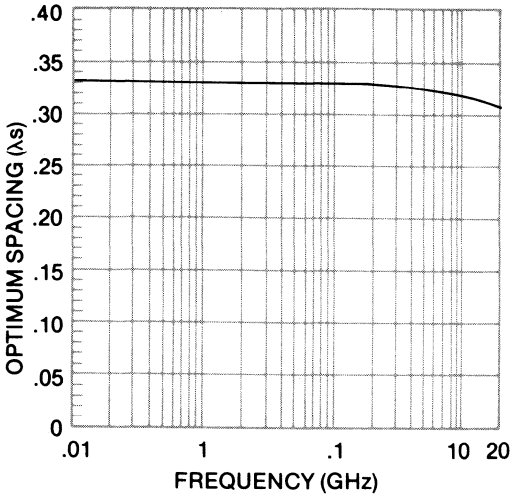


FIGURE 10.5-8 THREE ITERATED MA-4P102 SHUNT DIODE — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

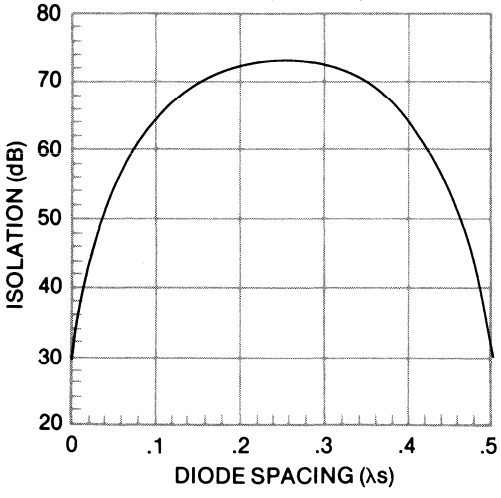


FIGURE 10.5-9 THREE SHUNT-ITERATED MA-4P102 DIODES — ISOLATION VS SPACING

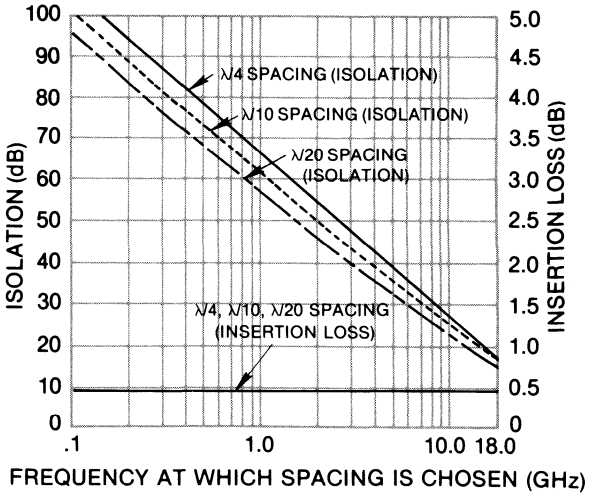


FIGURE 10.5-10 TWO SERIES-ITERATED MA-4P102 DIODES — λ/4, λ/10 AND λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

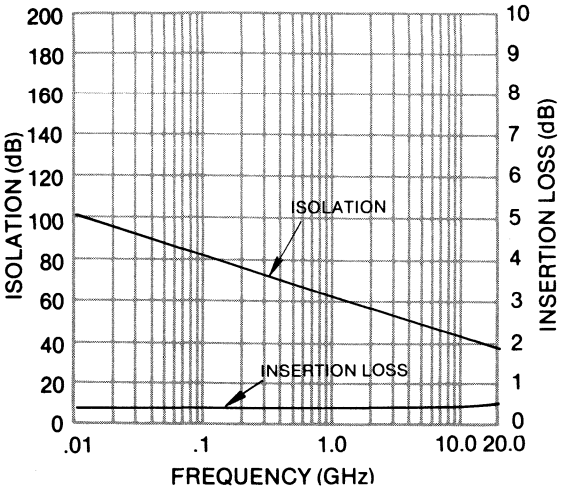


FIGURE 10.5-11 SPDT PARALLEL-SERIES MA-4P102 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

PIN specification and switch performance selection guide

104

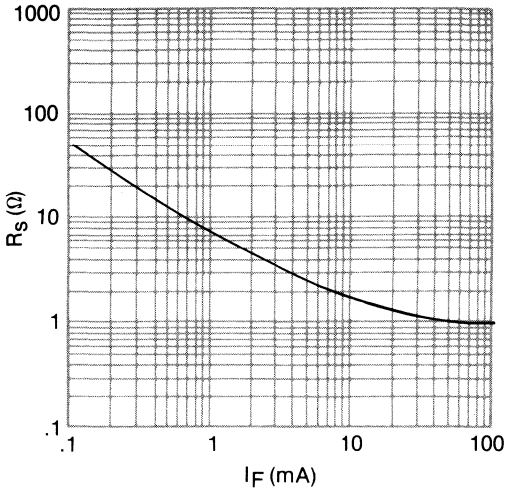
10.6 MA-4P103 SPECIFICATIONS AND SWITCHING PERFORMANCE

Voltage Breakdown (V_b)	=	30 volts (MIN) @ 10μA
Junction Capacitance (C_j)	=	.15 pF (MAX) @ 10 volts
Series Resistance (R_S)	=	1.5Ω (MAX) @ 20 mA
Carrier Lifetime (τ_L)	=	10 ns (TYP)
Reverse Recovery Time (T_{rr})	=	1.0 ns (TYP)
Thermal Resistance (θ_{jC})	=	40°C/W (MAX)
Power Dissipation @ 25°C	=	3.75W (MAX)
Standard Case Styles[1]	=	30, 54 and 134

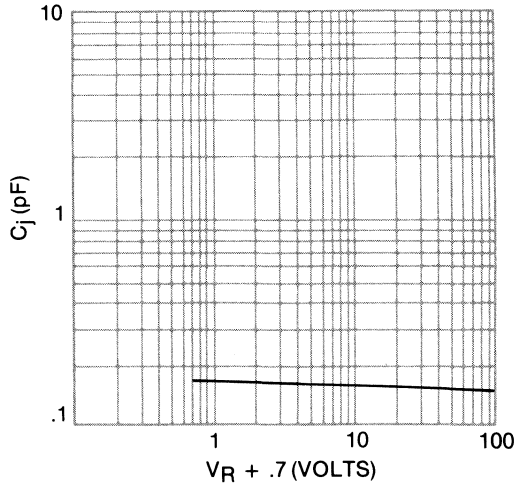
The MA-4P103 PIN diode features low series resistance and is designed for use as a low level limiter or ultra-fast switch. When used as a limiter, a limiting threshold of 40 mW is typical. These devices will handle 100 watts of pulsed power and 10 watts of CW power.

NOTE:

1. Custom packaging is available upon request.



SERIES RESISTANCE (R_S) VS FORWARD CURRENT (I_F) FOR AN MA-4P103 PIN DIODE



JUNCTION CAPACITANCE (C_j) VS REVERSE VOLTAGE (V_R) FOR AN MA-4P103 PIN DIODE

PIN specification and switch performance selection guide

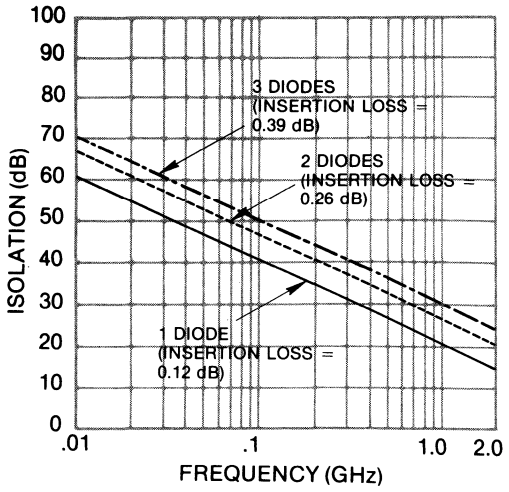


FIGURE 10.6-1 MA-4P103 SERIES DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

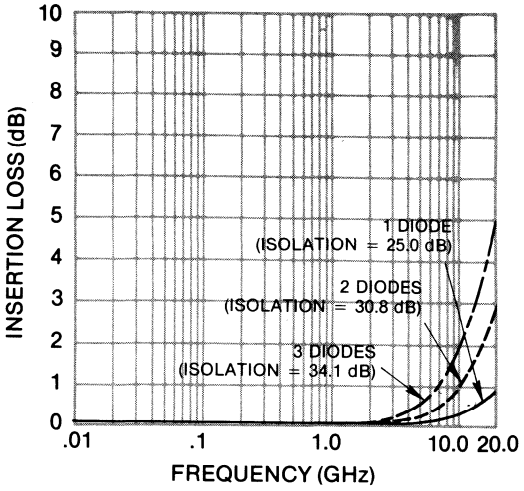


FIGURE 10.6-2 MA-4P103 SHUNT DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

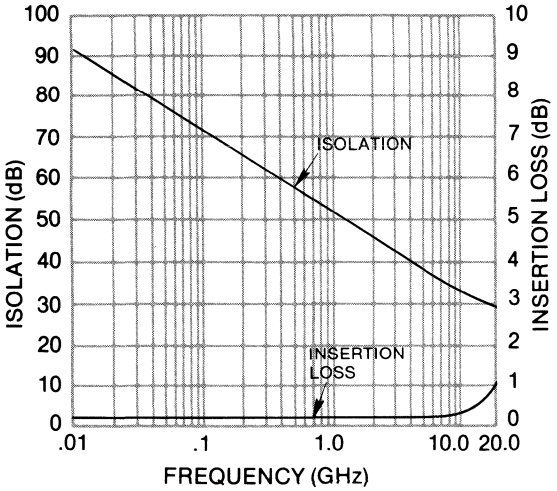


FIGURE 10.6-3 PARALLEL-SERIES MA-4P103 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

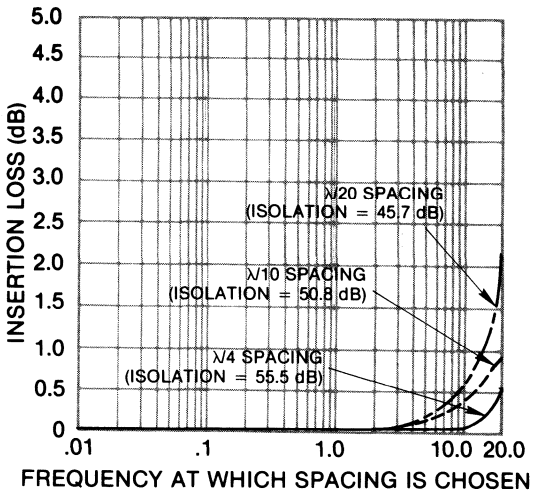


FIGURE 10.6-4 TWO SHUNT-ITERATED MA-4P103 DIODES — λ/4, λ/10 AND λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

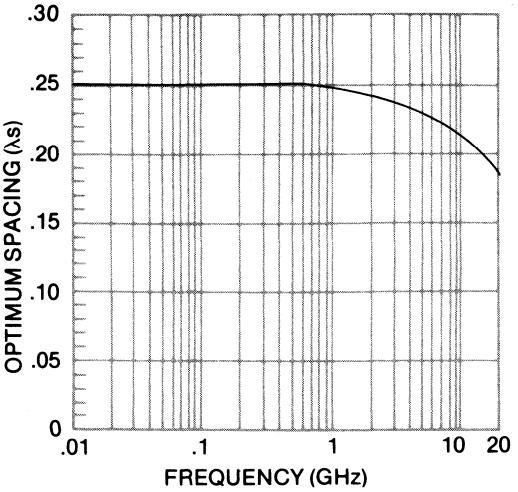


FIGURE 10.6-5 TWO ITERATED MA-4P103 SHUNT DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

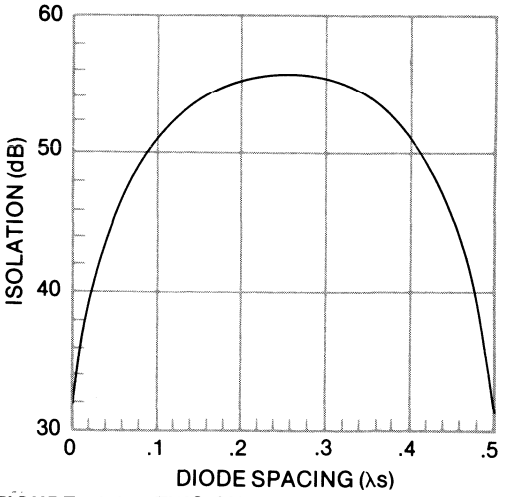


FIGURE 10.6-6 TWO SHUNT-ITERATED MA-4P103 DIODES — ISOLATION VS SPACING

PIN specification and switch performance selection guide

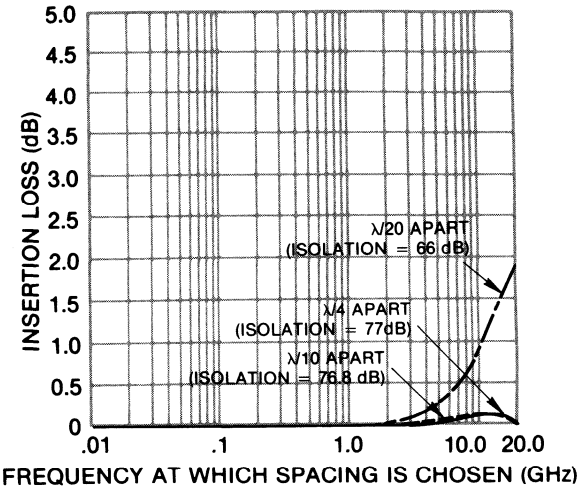


FIGURE 10.6-7 THREE SHUNT-ITERATED MA-4P103 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

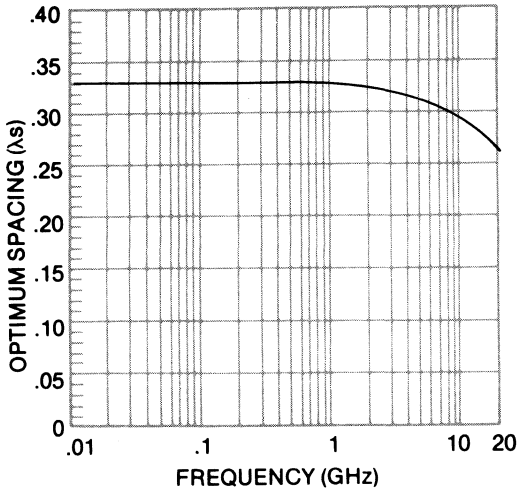


FIGURE 10.6-8 THREE SHUNT-ITERATED MA-4P103 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

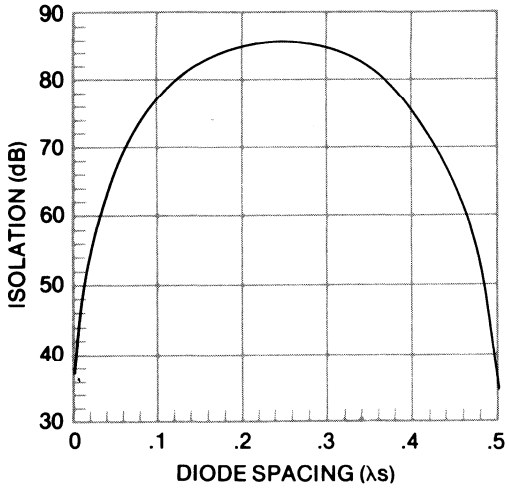


FIGURE 10.6-9 THREE SHUNT-ITERATED MA-4P103 DIODES — ISOLATION VS SPACING

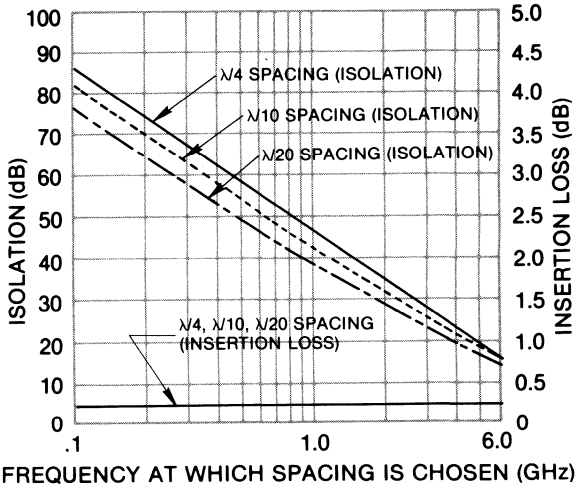


FIGURE 10.6-10 TWO SERIES-ITERATED MA-4P103 DIODES — λ/4, λ/10, λ/20 APART ISOLATION AND INSERTION LOSS VS FREQUENCY

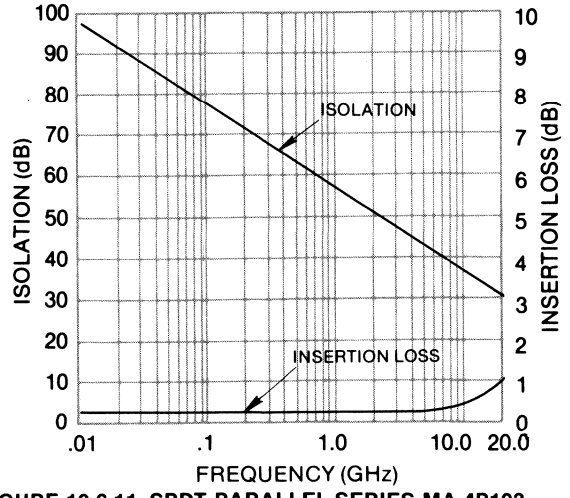


FIGURE 10.6-11 SPDT PARALLEL-SERIES MA-4P103 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

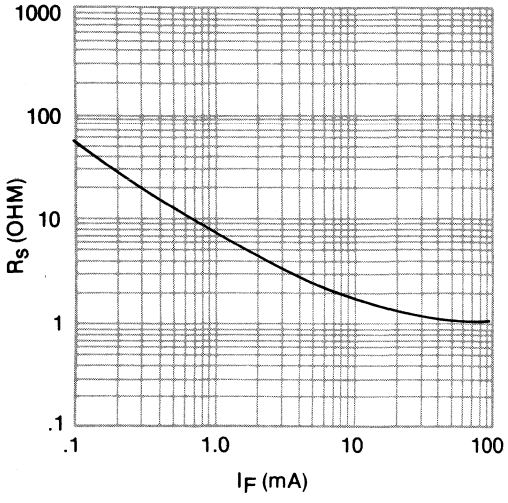
PIN specification and switch performance selection guide

10.7 MA-4P202 SPECIFICATIONS AND SWITCHING PERFORMANCE

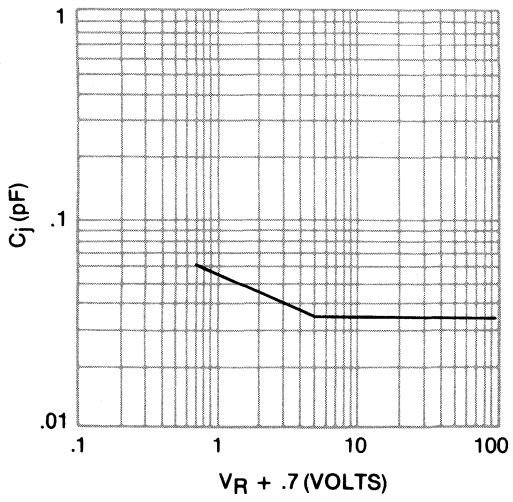
Voltage Breakdown (V_b)	=	100 volts (MIN) @ 10μA
Junction Capacitance (C_j)	=	.05 pF (MAX) @ 10 volts
Series Resistance (R_S)	=	2.0Ω (MAX) @ 10 mA
Carrier Lifetime (τ_L)	=	.100μs (TYP)
Reverse Recovery Time (T_{rr})	=	5 ns (TYP)
Thermal Resistance (θ_{jC})	=	60°C/W (MAX)
Power Dissipation @ 25°C	=	2.5W (MAX)
Standard Case Styles[1]	=	30, 54 and 134

The MA-4P202 PIN diode is specifically designed as a very low capacitance, general purpose fast switching diode. Switching times of 10 ns are typical. This low power device permits high frequency operation at very broad bandwidths.

NOTE:
1. Custom packaging is available upon request.



SERIES RESISTANCE (R_S) VS FORWARD CURRENT (I_F) FOR AN MA-4P202 PIN DIODE



JUNCTION CAPACITANCE (C_j) VS REVERSE VOLTAGE (V_R) FOR AN MA-4P202 PIN DIODE

PIN specification and switch performance selection guide

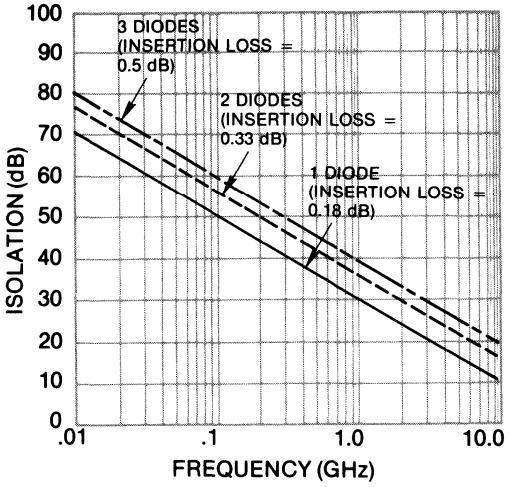


FIGURE 10.7-1 MA-4P202 SERIES DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

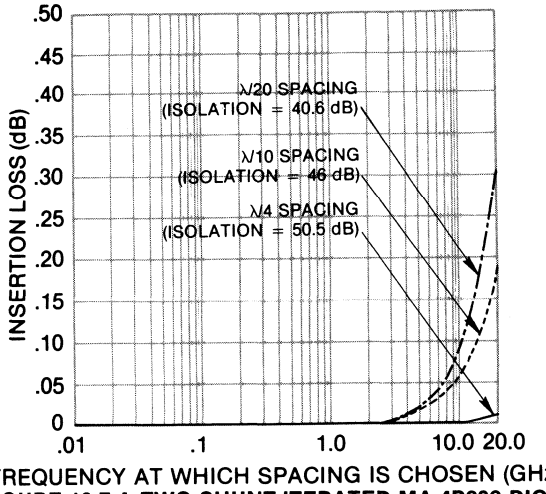


FIGURE 10.7-4 TWO SHUNT-ITERATED MA-4P202 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

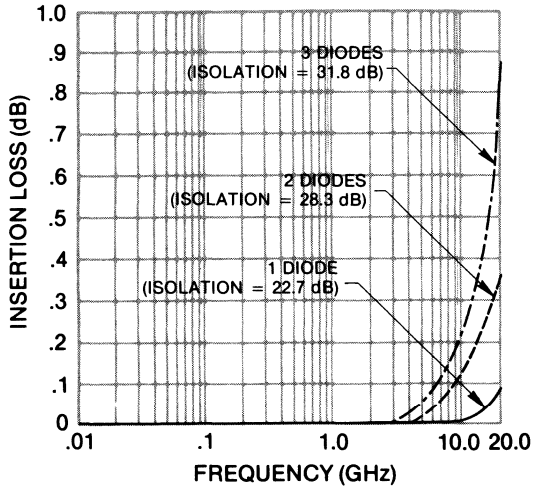


FIGURE 10.7-2 MA-4P202 SHUNT DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

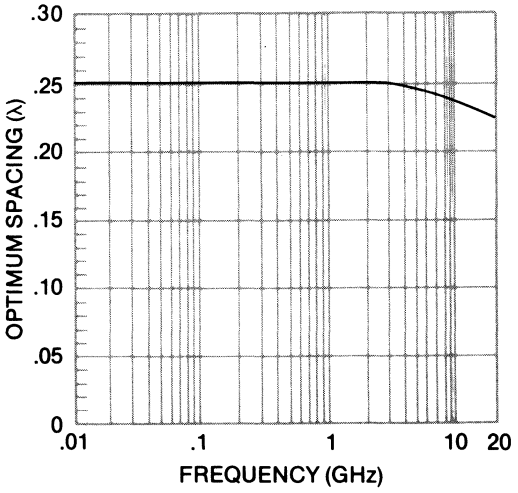


FIGURE 10.7-5 TWO SHUNT-ITERATED MA-4P202 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

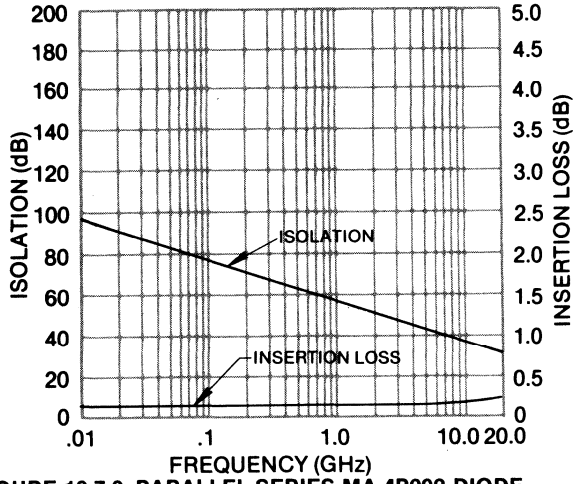


FIGURE 10.7-3 PARALLEL-SERIES MA-4P202 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

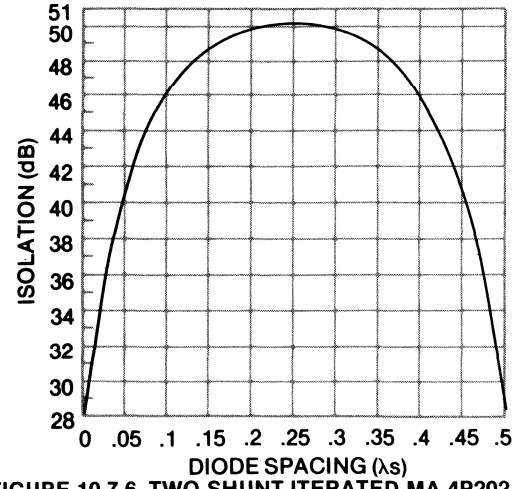


FIGURE 10.7-6 TWO SHUNT-ITERATED MA-4P202 DIODES — ISOLATION VS SPACING

PIN specification and switch performance selection guide

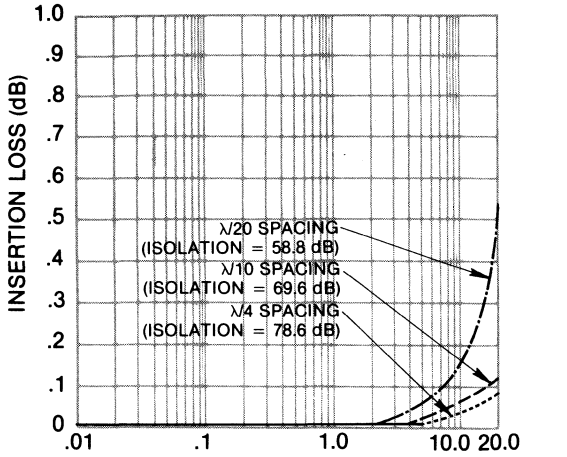


FIGURE 10.7-7 THREE SHUNT-ITERATED MA-4P202 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

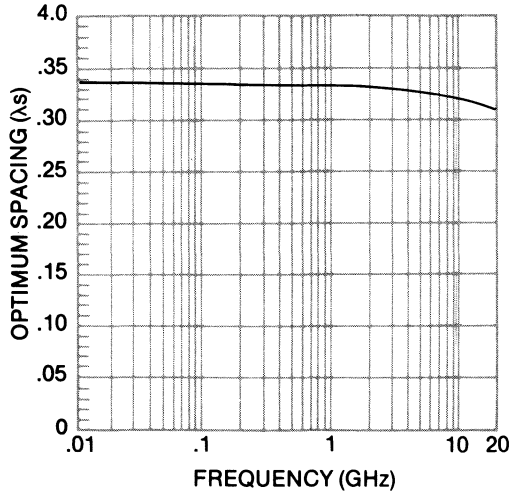


FIGURE 10.7-8 THREE SHUNT-ITERATED MA-4P202 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

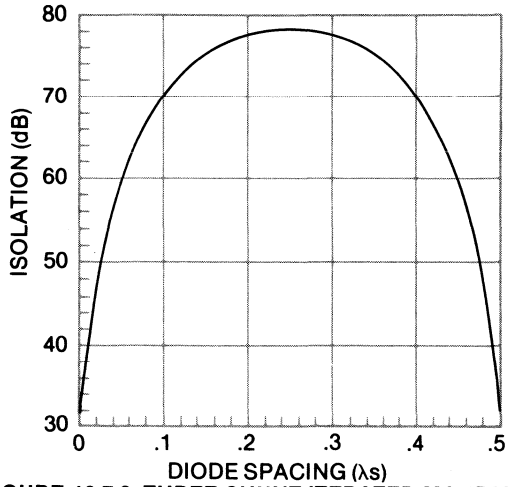


FIGURE 10.7-9 THREE SHUNT-ITERATED MA-4P202 DIODES — ISOLATION VS SPACING

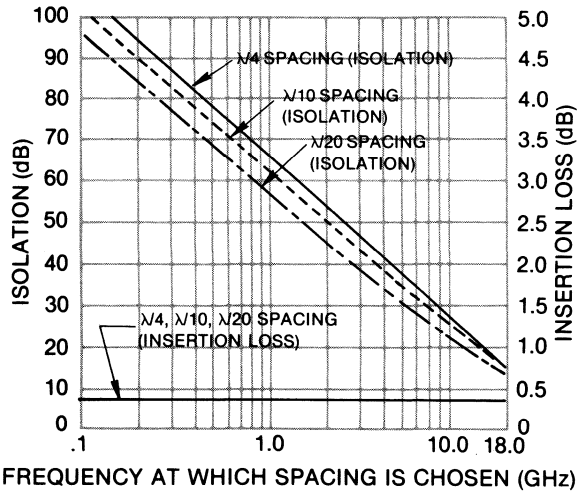


FIGURE 10.7-10 TWO SERIES ITERATED MA-4P202 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

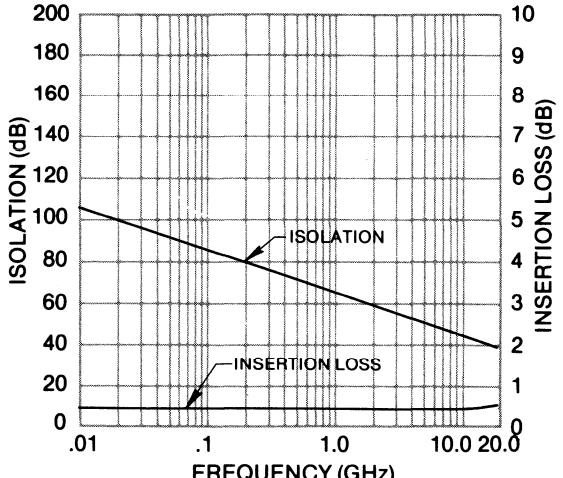


FIGURE 10.7-11 SPDT PARALLEL-SERIES MA-4P202 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

PIN specification and switch performance selection guide

110

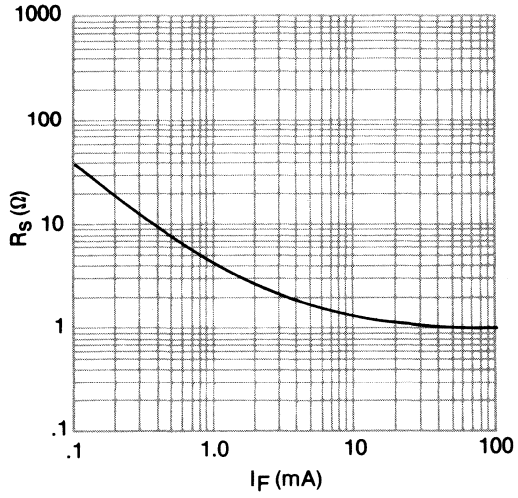
10.8 MA-4P203 SPECIFICATIONS AND SWITCHING PERFORMANCE

Voltage Breakdown (V_b)	= 100 volts (MIN) @ 10μA
Junction Capacitance (C_j)	= .15 pF (MAX) @ 10 volts
Series Resistance (R_S)	= 1.5Ω (MAX) @ 10 mA
Carrier Lifetime (τ_L)	= .100μs (TYP)
Reverse Recovery Time (T_{rr})	= 20 ns (TYP)
Thermal Resistance (θ_{jc})	= 30°C/W (MAX)
Power Dissipation @ 25°C	= 5.0W (MAX)
Standard Case Styles[1]	= 30, 54 and 134

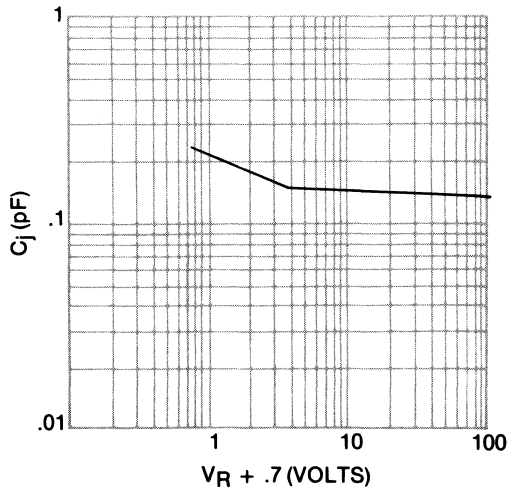
The MA-4P203 is the ultimate utility PIN diode. Designed to handle low power levels, this device typically has switching speeds of 10 ns and low series resistance for minimum loss in both fast switching and phase shift applications.

NOTE:

1. Custom packaging is available upon request.



SERIES RESISTANCE (R_S) VS FORWARD CURRENT (I_F) FOR AN MA-4P203 PIN DIODE



TYPICAL JUNCTION CAPACITANCE (C_j) VS REVERSE VOLTAGE (V_R) FOR AN MA-4P203 PIN DIODE

PIN specification and switch performance selection guide

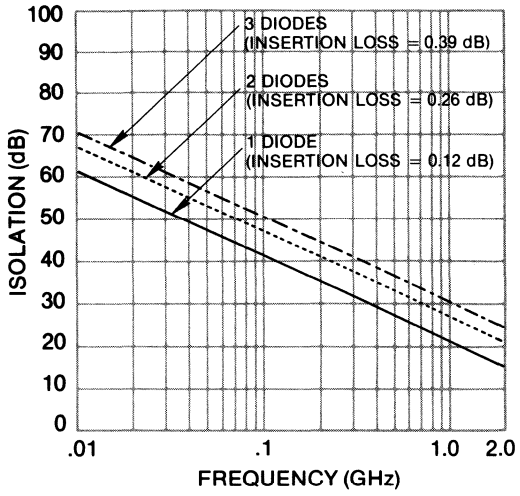


FIGURE 10.8-1 MA-4P203 SERIES DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

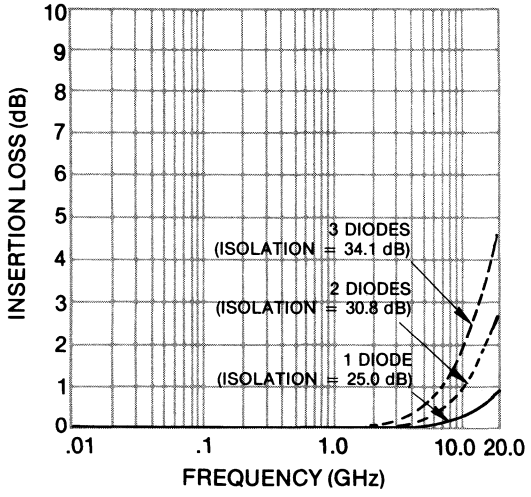


FIGURE 10.8-2 MA-4P203 SHUNT DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

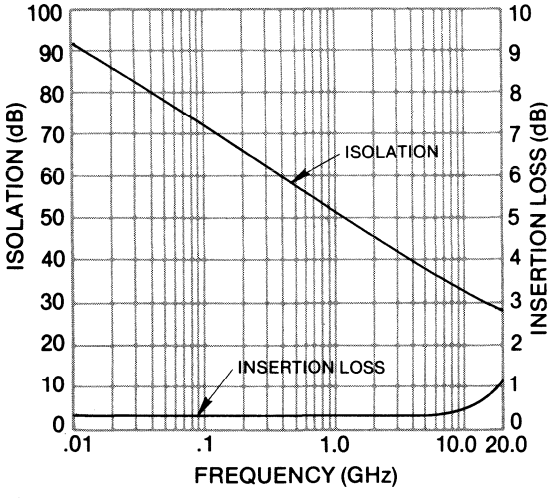


FIGURE 10.8-3 PARALLEL-SERIES MA-4P203 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

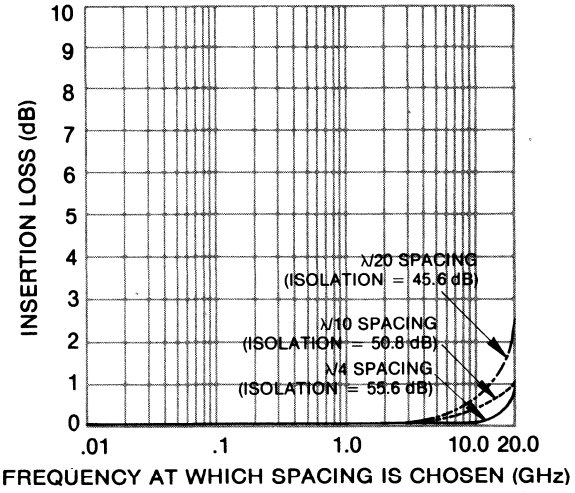


FIGURE 10.8-4 TWO SHUNT-ITERATED MA-4P203 DIODES — λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

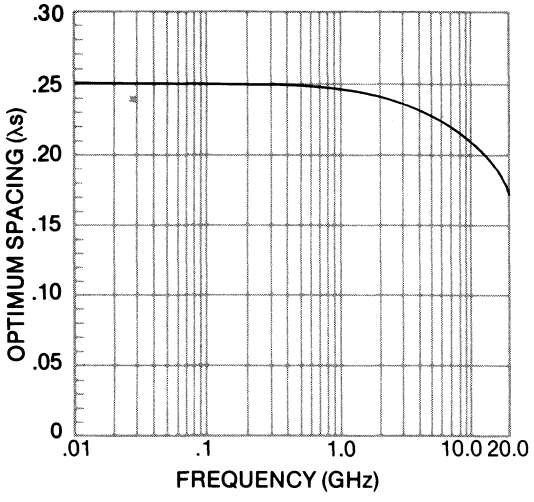


FIGURE 10.8-5 TWO SHUNT-ITERATED MA-4P203 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

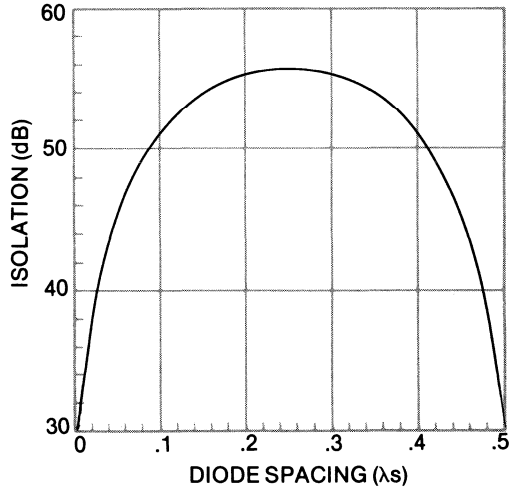


FIGURE 10.8-6 TWO SHUNT-ITERATED MA-4P203 DIODES — ISOLATION VS SPACING

PIN specification and switch performance selection guide

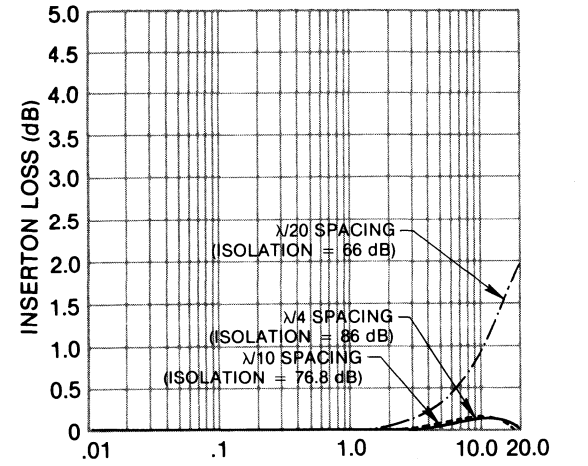


FIGURE 10.8-7 THREE SHUNT-ITERATED MA-4P203 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

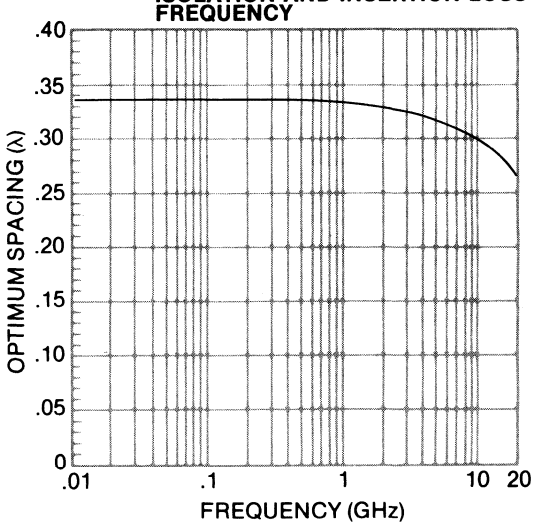


FIGURE 10.8-8 THREE SHUNT-ITERATED MA-4P203 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

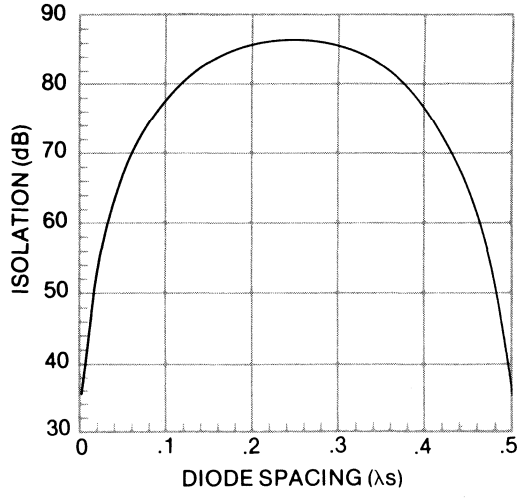


FIGURE 10.8-9 THREE SHUNT-ITERATED MA-4P203 DIODES — ISOLATION VS SPACING

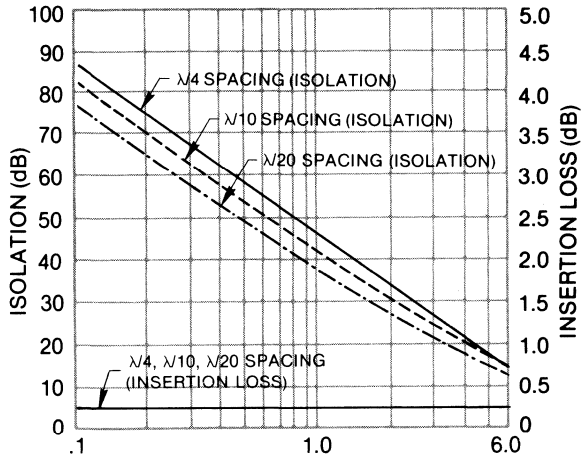


FIGURE 10.8-10 TWO SERIES-ITERATED MA-4P203 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

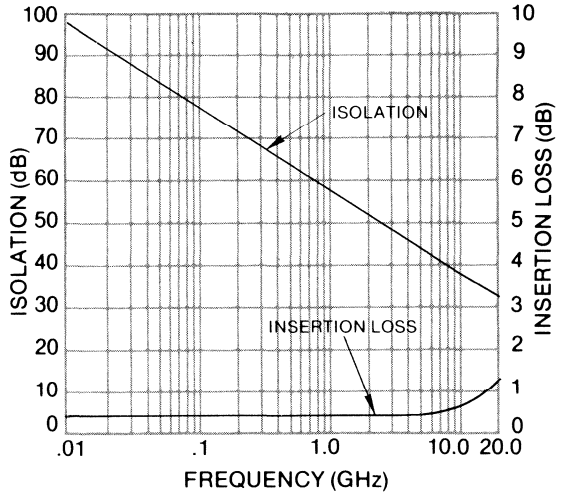


FIGURE 10.8-11 SPDT PARALLEL-SERIES MA-4P203 DIODE — ISOLATION AND INSERTION LOSS VS FREQUENCY

PIN specification and switch performance selection guide

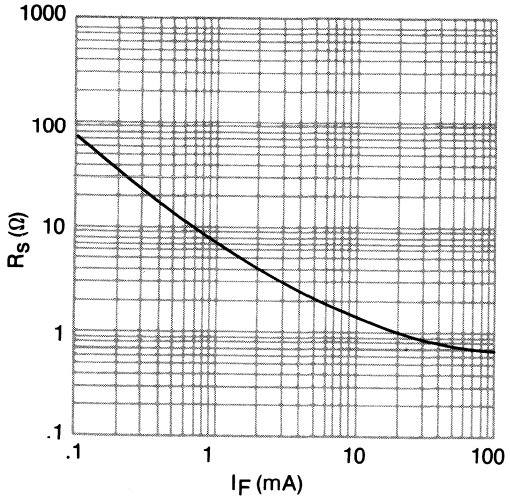
10.9 MA-4P303 SPECIFICATIONS AND SWITCHING PERFORMANCE

Voltage Breakdown (V_b)	=	200 volts (MIN) @ 10μA
Junction Capacitance (C_j)	=	.15 pF (MAX) @ 10 volts
Series Resistance (R_S)	=	1.5Ω (MAX) @ 10 mA
Carrier Lifetime (τ_L)	=	.200μs (TYP)
Reverse Recovery Time (T_{rr})	=	65 ns (TYP)
Thermal Resistance (θ_{jc})	=	30°C/W (MAX)
Power Dissipation @ 25°C	=	5.0W (MAX)
Standard Case Styles[1]	=	30, 54 and 134

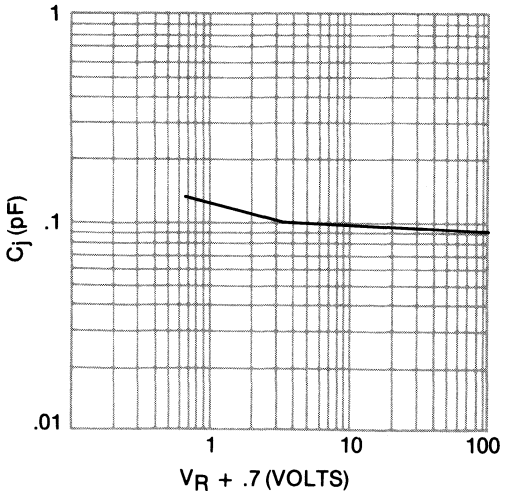
The MA-4P303 PIN diode is a low-power, general purpose switching or phase shifter device. This diode is designed with an optimum R_S, C_j tradeoff for low-loss and broadband operation.

NOTE:

1. Custom packaging is available upon request.



SERIES RESISTANCE (R_S) VS FORWARD CURRENT (I_F) FOR AN MA-4P303 PIN DIODE



JUNCTION CAPACITANCE (C_j) VS REVERSE VOLTAGE (V_R) FOR AN MA-4P303 PIN DIODE

PIN specification and switch performance selection guide

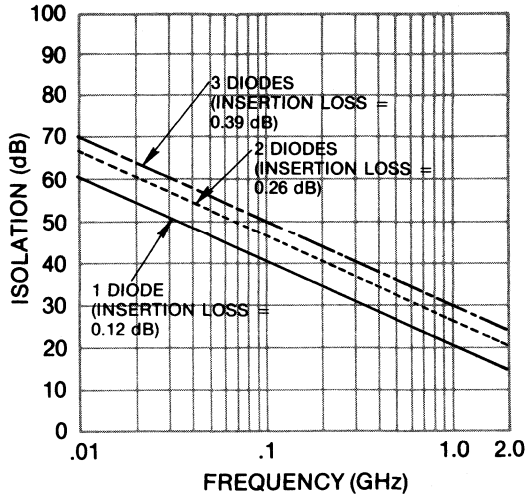


FIGURE 10.9-1 MA-4P303 SERIES DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

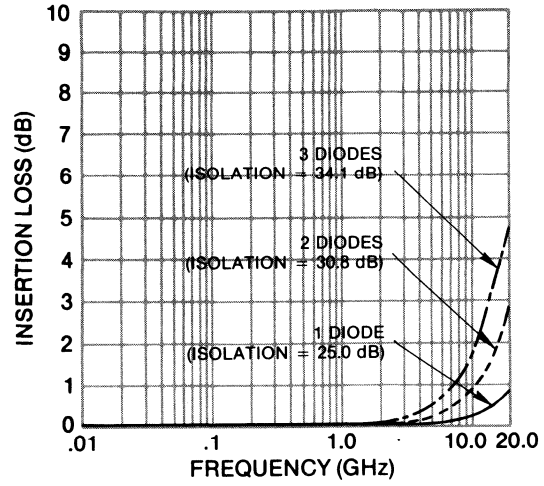


FIGURE 10.9-2 MA-4P303 SHUNT DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

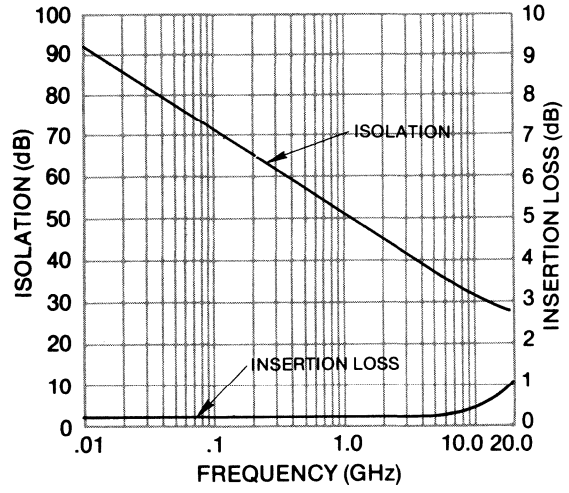


FIGURE 10.9-3 PARALLEL-SERIES MA-4P303 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

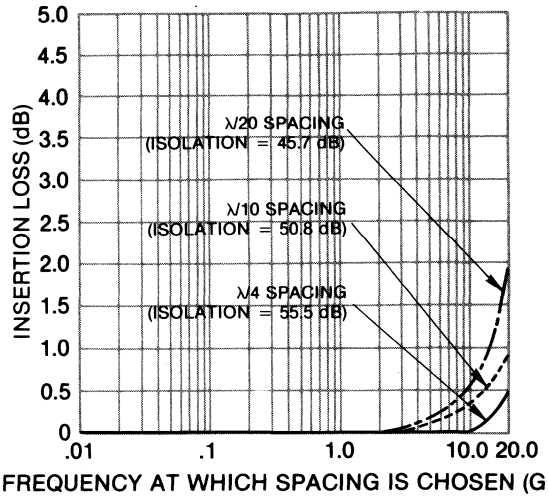


FIGURE 10.9-4 TWO SHUNT-ITERATED MA-4P303 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

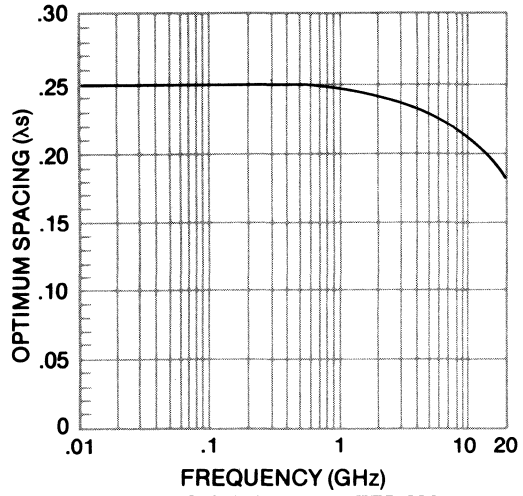


FIGURE 10.9-5 TWO SHUNT-ITERATED MA-4P303 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

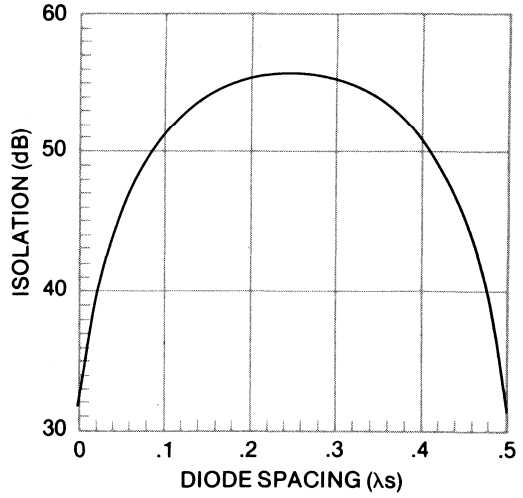


FIGURE 10.9-6 TWO SHUNT-ITERATED MA-4P303 DIODES — ISOLATION VS SPACING

PIN specification and switch performance selection guide

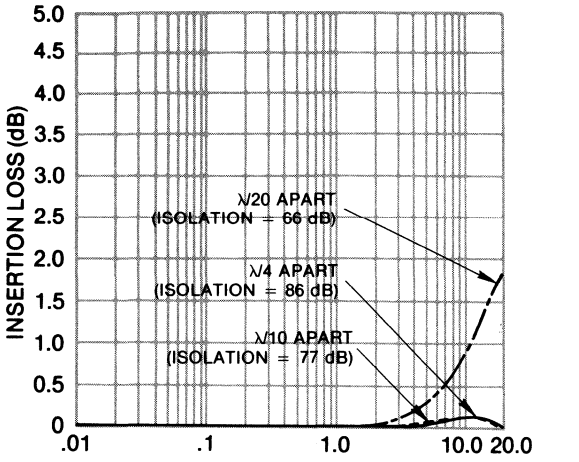


FIGURE 10.9-7 THREE SHUNT-ITERATED MA-4P303 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

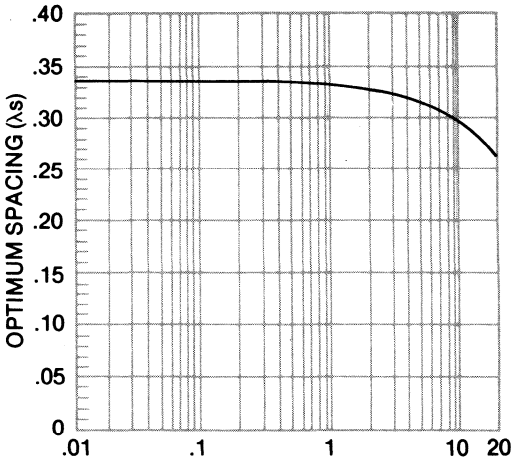


FIGURE 10.9-8 THREE SHUNT-ITERATED MA-4P303 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

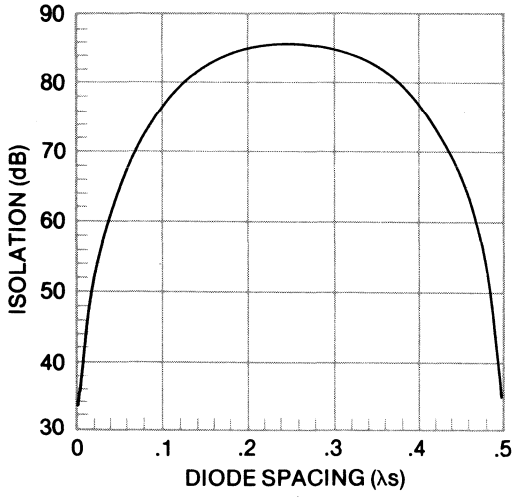


FIGURE 10.9-9 THREE SHUNT-ITERATED MA-4P303 DIODES — ISOLATION VS SPACING

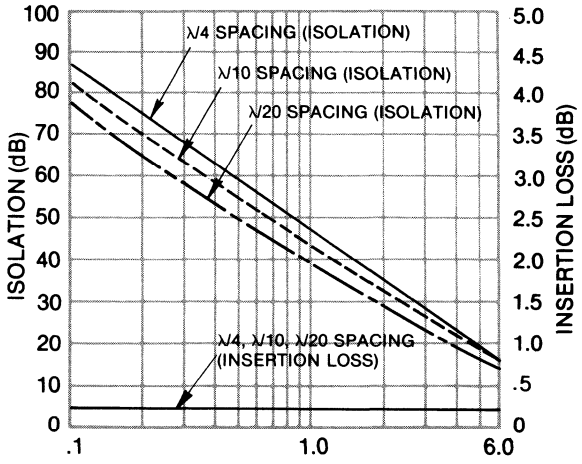


FIGURE 10.9-10 TWO SERIES-ITERATED MA-4P303 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

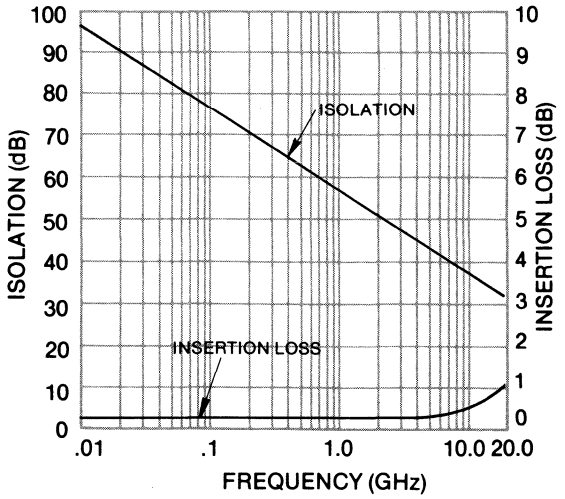


FIGURE 10.9-11 SPDT PARALLEL-SERIES MA-4P303 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

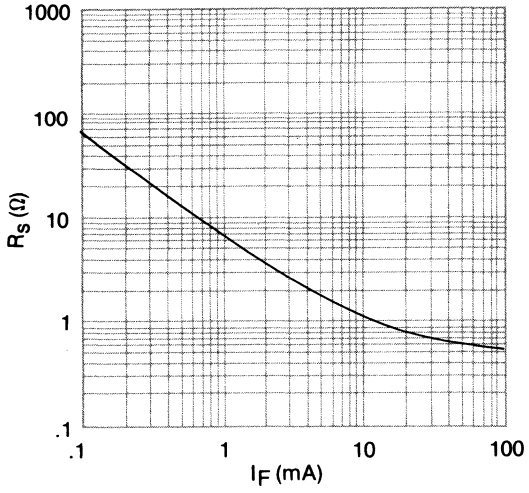
PIN specification and switch performance selection guide

10.10 MA-4P404 SPECIFICATIONS AND SWITCHING PERFORMANCE

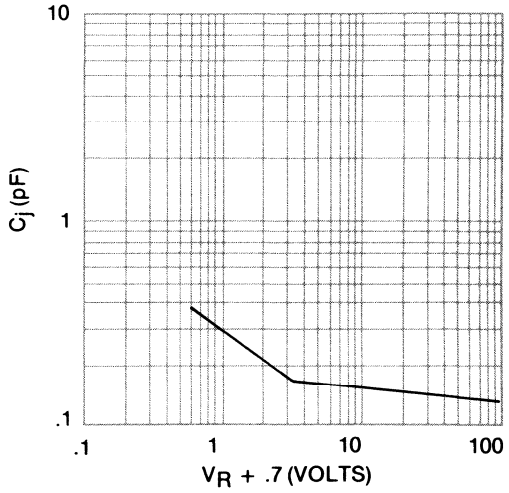
Voltage Breakdown (V_b)	=	300 volts (MIN) @ 10μA
Junction Capacitance (C_j)	=	.20 pF (MAX) @ 50 volts
Series Resistance (R_S)	=	0.6Ω (MAX) @ 50 mA
Carrier Lifetime (τ_L)	=	1.0μs (TYP)
Reverse Recovery Time (T_{rr})	=	.140 μs (TYP)
Thermal Resistance (θ_{jC})	=	20°C/W (MAX)
Power Dissipation @ 25°C	=	7.5W (MAX)
Standard Case Styles[1]	=	30, 54 and 134

The MA-4P404 PIN diode is specifically designed for use as a moderate power switching device. This diode's 300 volt minimum breakdown voltage allows for greater power handling capability than lower capacitance diodes, but with a typical switching speed of only 100 ns. Rapid switching at moderate power levels is featured here.

NOTE:
1. Custom packaging is available upon request.



SERIES RESISTANCE (R_S) VS FORWARD CURRENT (I_F) FOR AN MA-4P404 PIN DIODE



JUNCTION CAPACITANCE (C_j) VS REVERSE VOLTAGE (V_R) FOR AN MA-4P404 PIN DIODE

PIN specification and switch performance selection guide

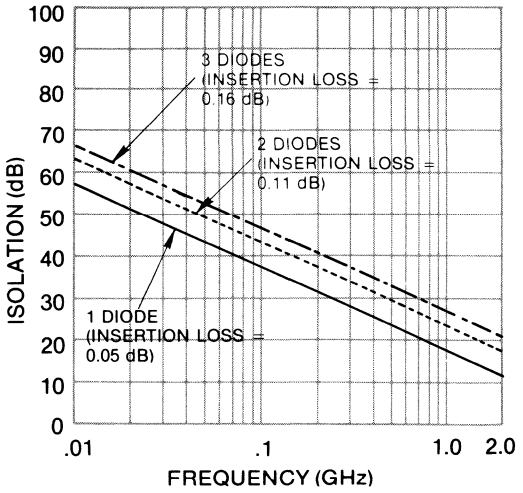


FIGURE 10.10-1 MA-4P404 SERIES DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

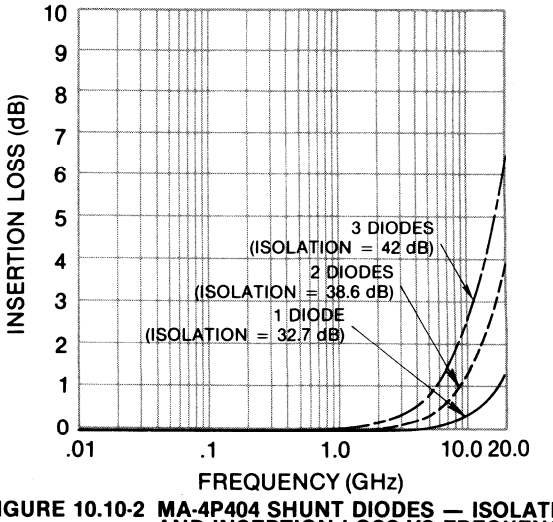


FIGURE 10.10-2 MA-4P404 SHUNT DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

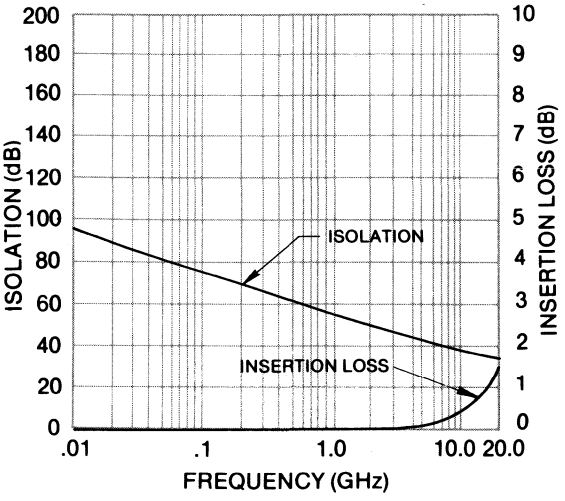


FIGURE 10.10-3 PARALLEL-SERIES MA-4P404 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

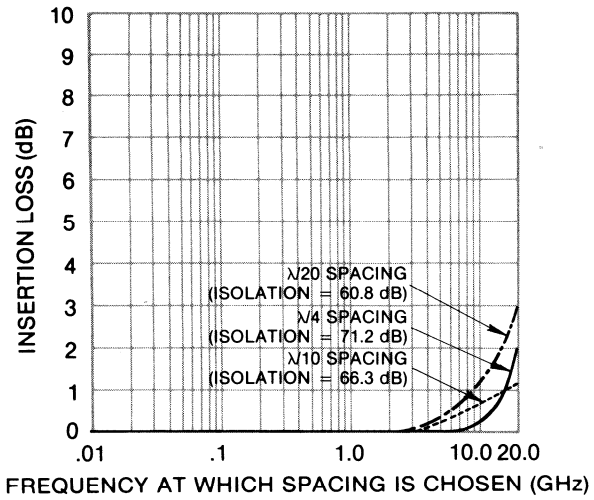


FIGURE 10.10-4 TWO SHUNT-ITERATED MA-4P404 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

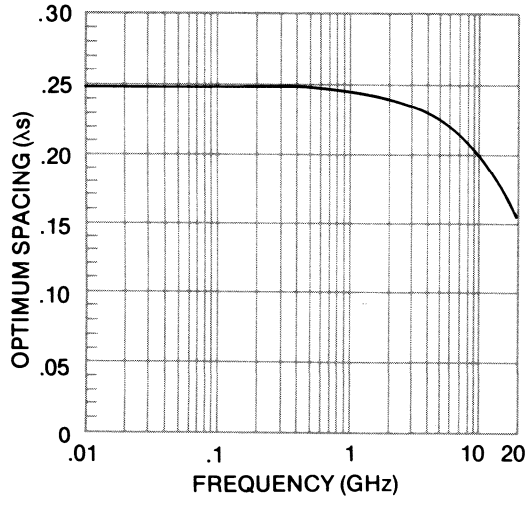


FIGURE 10.10-5 TWO SHUNT-ITERATED MA-4P404 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

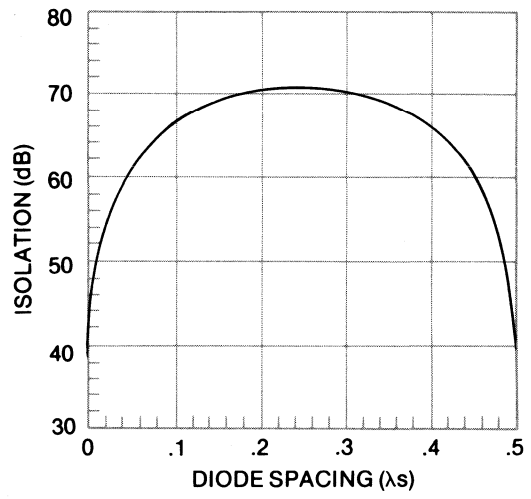


FIGURE 10.10-6 TWO SHUNT-ITERATED MA-4P404 DIODES — ISOLATION VS SPACING

PIN specification and switch performance selection guide

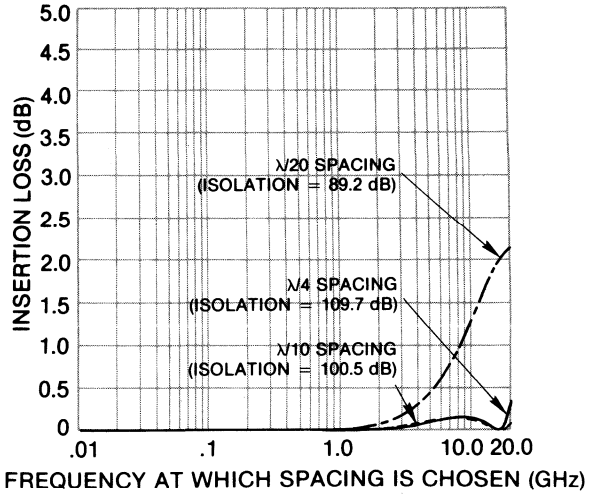


FIGURE 10.10-7 THREE SHUNT-ITERATED MA-4P404 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

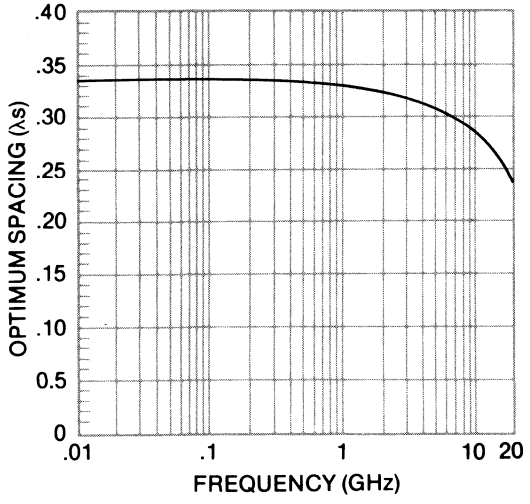


FIGURE 10.10-8 THREE SHUNT-ITERATED MA-4P404 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

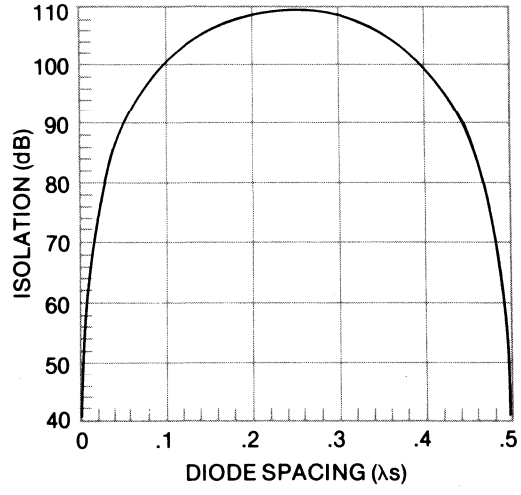


FIGURE 10.10-9 THREE SHUNT-ITERATED MA-4P404 DIODES — ISOLATION VS SPACING

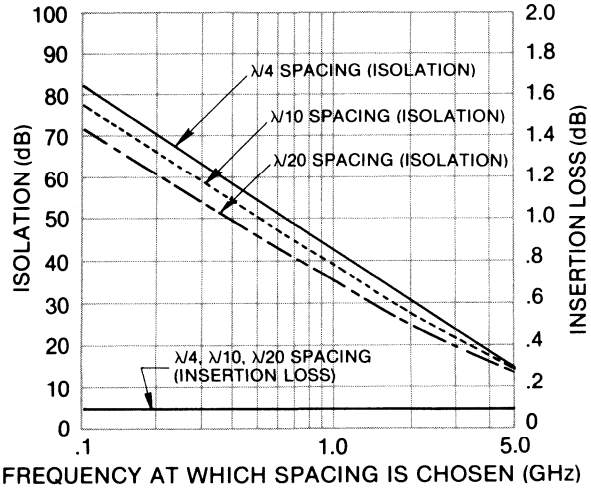


FIGURE 10.10-10 TWO SERIES-ITERATED MA-4P404 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

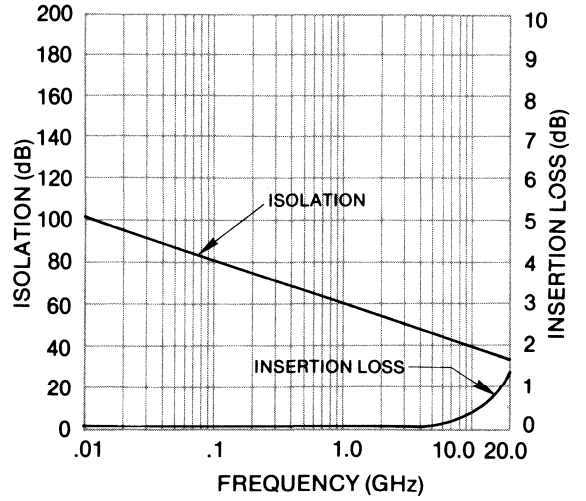


FIGURE 10.10-11 SPDT PARALLEL-SERIES MA-4P404 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

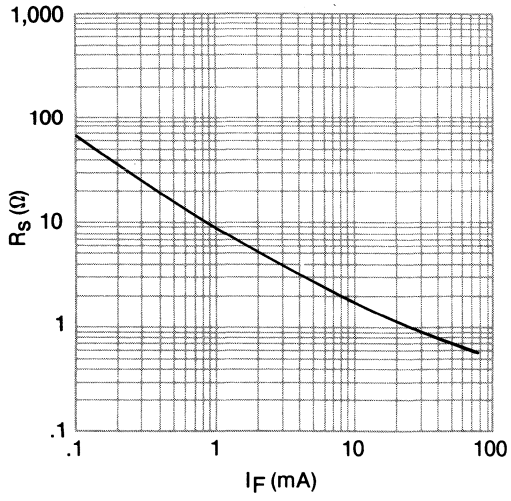
PIN specification and switch performance selection guide

10.11 MA-4P504 SPECIFICATIONS AND SWITCHING PERFORMANCE

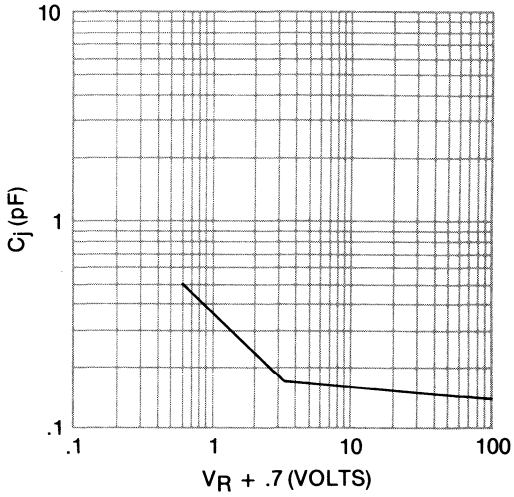
Voltage Breakdown (V_b)	=	500 volts (MIN) @ 10μA
Junction Capacitance (C_j)	=	.20 pF (MAX) @ 100 volts
Series Resistance (R_S)	=	0.6Ω (MAX) @ 100 mA
Carrier Lifetime (τ_L)	=	2.0μs (TYP)
Reverse Recovery Time (T_{rr})	=	.350 μs (TYP)
Thermal Resistance (θ_{jC})	=	20°C/W (MAX)
Power Dissipation @ 25°C	=	7.5W (MAX)
Standard Case Styles[1]	=	30, 4 and 131[2]

The MA-4P504 PIN diode is a moderate to high power switching diode whose R_S and C_j have been optimized for low power dissipation and loss at moderate frequencies. Switching speeds of 200 ns are typical for this device, CERMACHIP™ construction is standard.

NOTES:
1. Custom packaging is available upon request.
2. Case style 131 is a CERMACHIP™ (hermetically sealed chip).



SERIES RESISTANCE (R_S) VS FORWARD CURRENT (I_F) FOR AN MA-4P504 PIN DIODE



JUNCTION CAPACITANCE (C_j) VS REVERSE VOLTAGE (V_R) FOR AN MA-4P504 PIN DIODE

PIN specification and switch performance selection guide

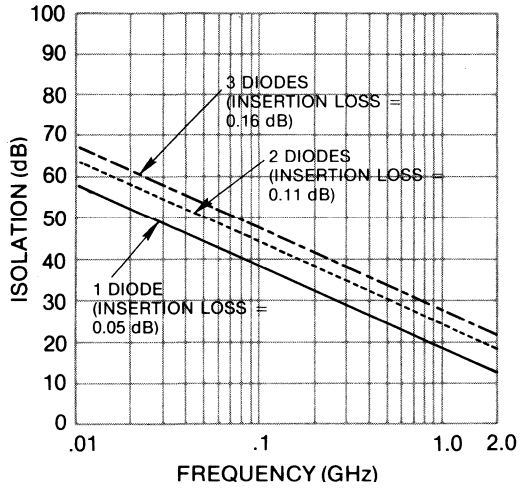


FIGURE 10.11-1 MA-4P504 SERIES DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

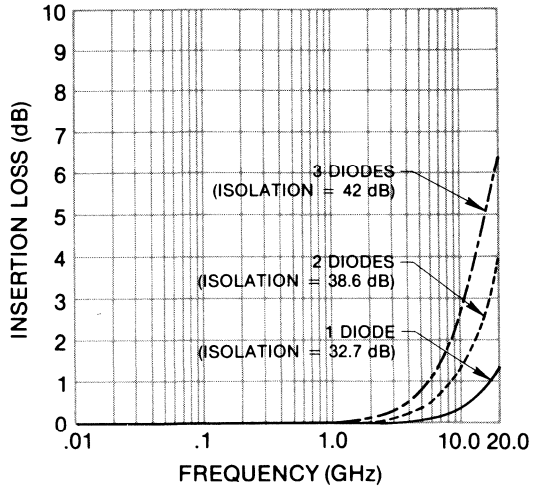


FIGURE 10.11-2 MA-4P504 SHUNT DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

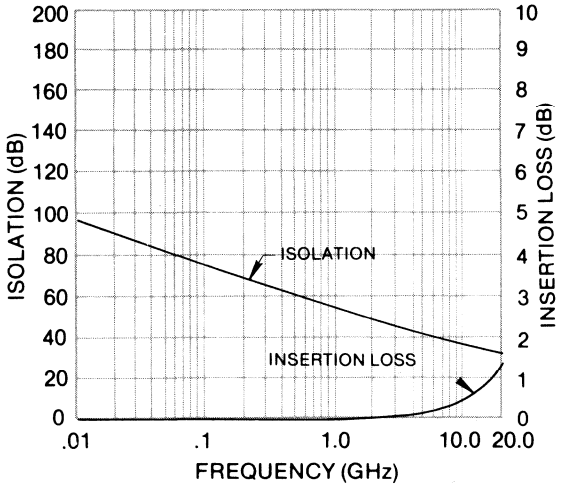


FIGURE 10.11-3 PARALLEL-SERIES MA-4P504 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

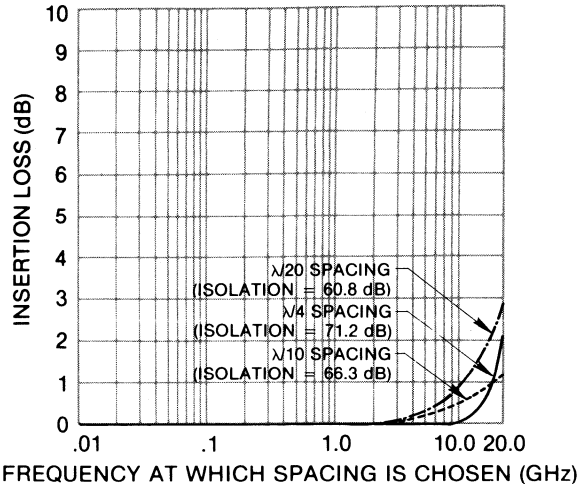


FIGURE 10.11-4 TWO SHUNT-ITERATED MA-4P504 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

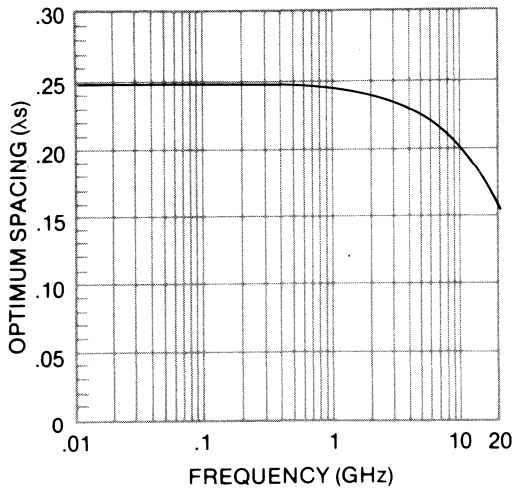


FIGURE 10.11-5 TWO SHUNT-ITERATED MA-4P504 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

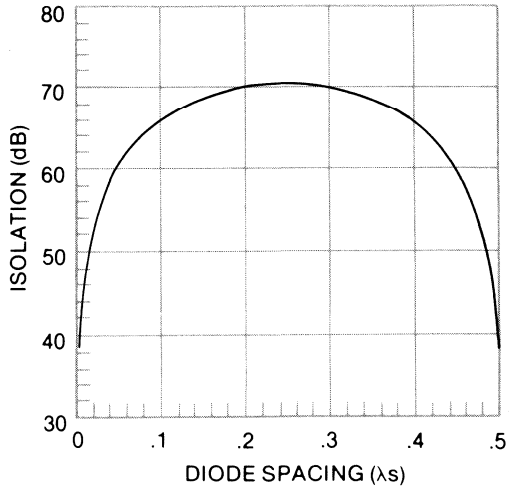


FIGURE 10.11-6 TWO SHUNT-ITERATED MA-4P504 DIODES — ISOLATION VS SPACING

PIN specification and switch performance selection guide

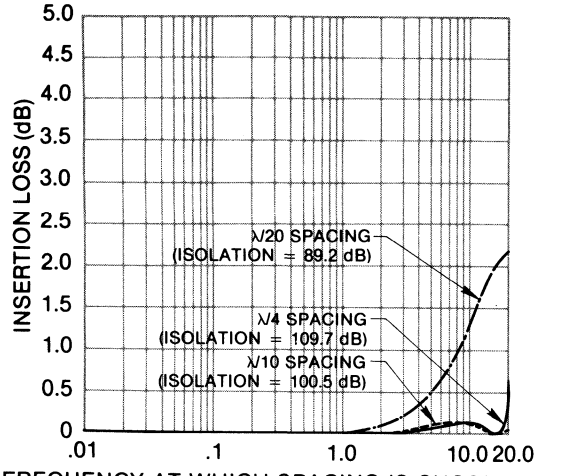


FIGURE 10.11-7 THREE SHUNT-ITERATED MA-4P504 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

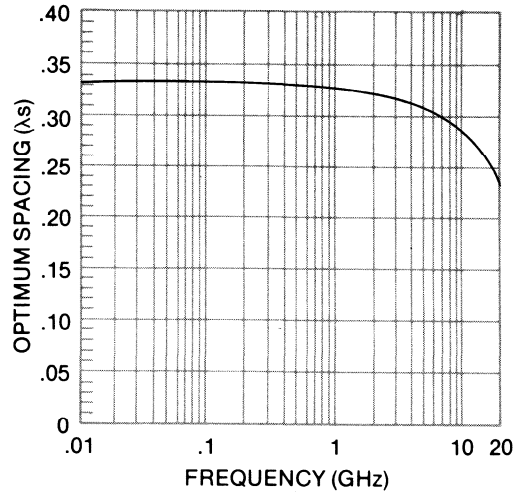


FIGURE 10.11-8 THREE SHUNT-ITERATED MA-4P504 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

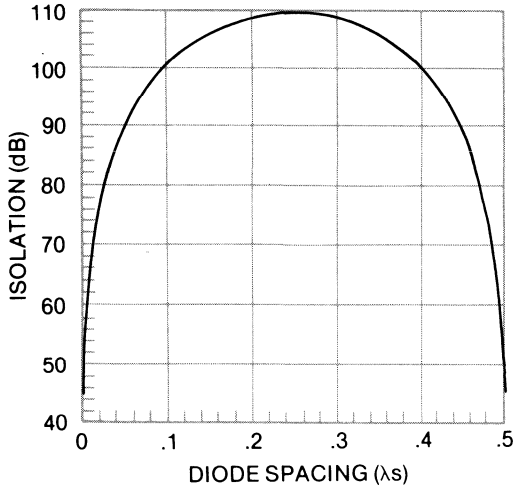


FIGURE 10.11-9 THREE SHUNT-ITERATED MA-4P504 DIODES — ISOLATION VS SPACING

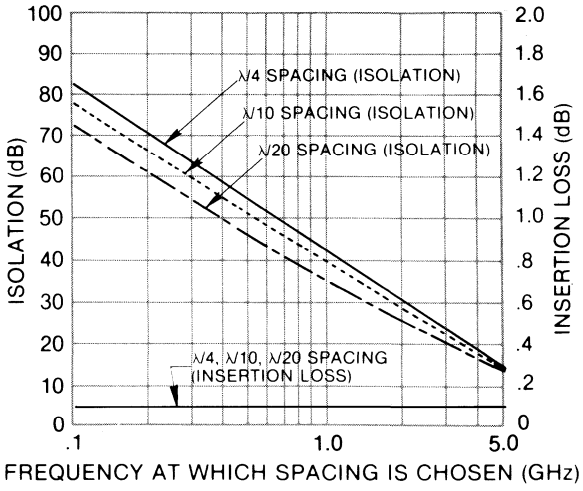


FIGURE 10.11-10 TWO SERIES-ITERATED MA-4P504 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

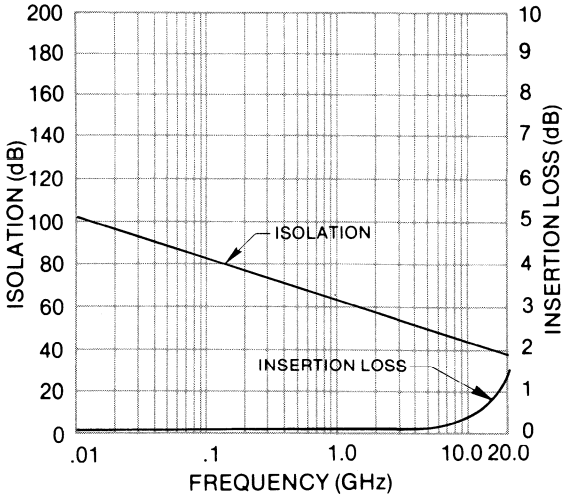


FIGURE 10.11-11 SPDT PARALLEL-SERIES MA-4P504 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

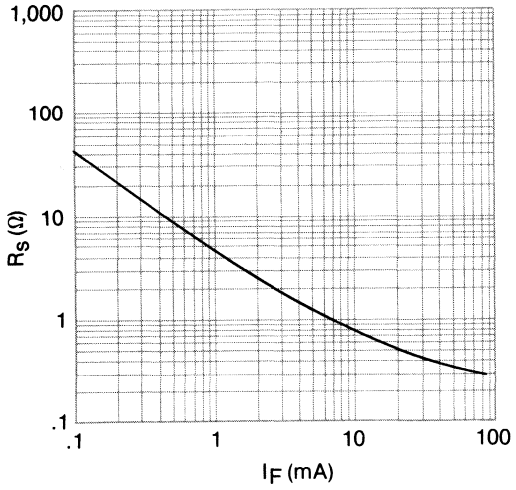
PIN specification and switch performance selection guide

10.12 MA-4P505 SPECIFICATIONS AND SWITCHING PERFORMANCE

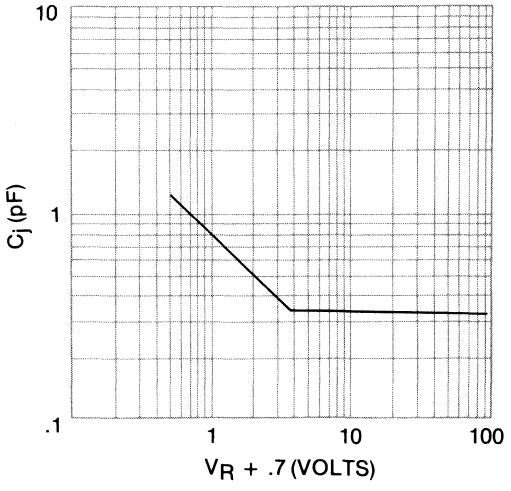
Voltage Breakdown (V_b)	=	500 volts (MIN) @ 10μA
Junction Capacitance (C_j)	=	.35 pF (MAX) @ 100 volts
Series Resistance (R_S)	=	.45Ω (MAX) @ 100 mA
Carrier Lifetime (τ_L)	=	2.0μs (TYP)
Reverse Recovery Time (T_{rr})	=	.350 μs (TYP)
Thermal Resistance (θ_{jC})	=	15°C/W (MAX)
Power Dissipation @ 25°C	=	10W (MAX)
Standard Case Styles[1]	=	30, 4 and 131[2]

The MA-4P505 PIN diode is intended for moderate to high power switching applications. Typical switching speeds of 200 nsec and low values of junction capacitance make this device an ideal rapid switching, moderate power, high frequency choice in switching diodes. Each diode features CERMACHIP™ construction.

NOTES:
1. Custom packaging is available upon request.
2. Case style 131 is a CERMACHIP™ (hermetically sealed chip).



SERIES RESISTANCE (R_S) VS FORWARD CURRENT (I_F) FOR AN MA-4P505 PIN DIODE



JUNCTION CAPACITANCE (C_j) VS REVERSE VOLTAGE (V_R) FOR AN MA-4P505 PIN DIODE

PIN specification and switch performance selection guide

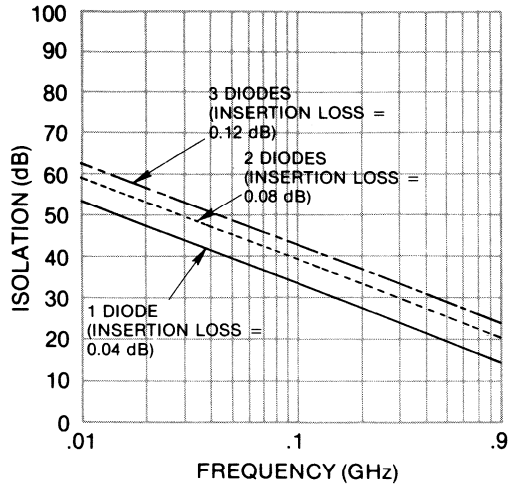


FIGURE 10.12-1 MA-4P505 SERIES DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

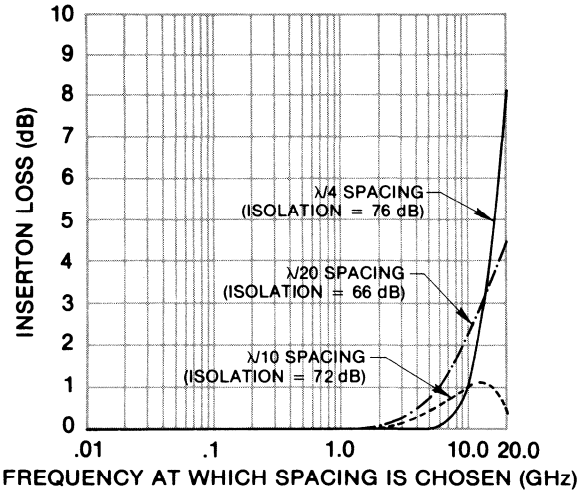


FIGURE 10.12-4 TWO SHUNT-ITERATED MA-4P505 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

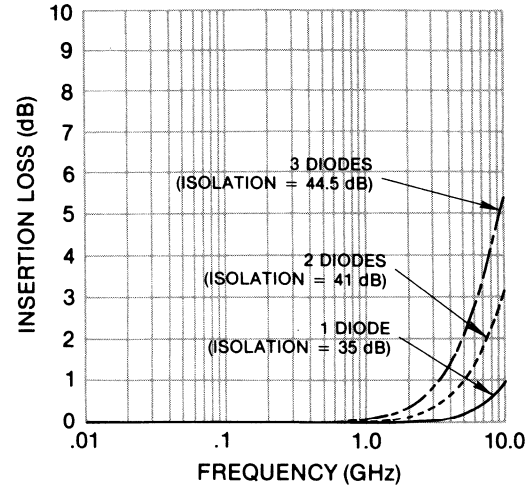


FIGURE 10.12-2 MA-4P505 SHUNT DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

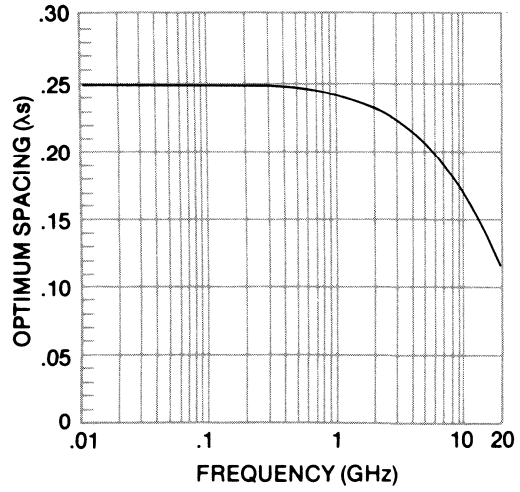


FIGURE 10.12-5 TWO SHUNT-ITERATED MA-4P505 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

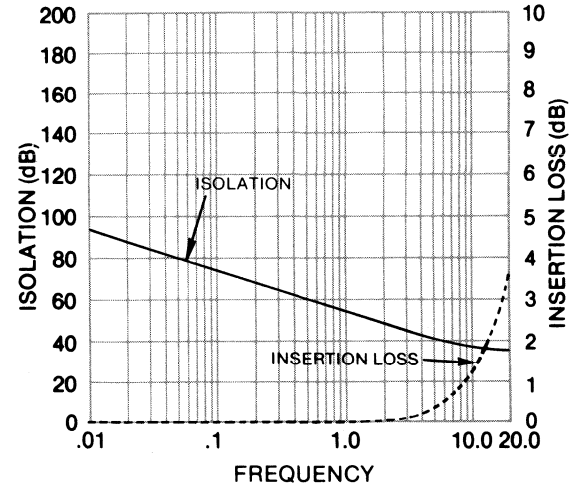


FIGURE 10.12-3 PARALLEL-SERIES MA-4P505 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

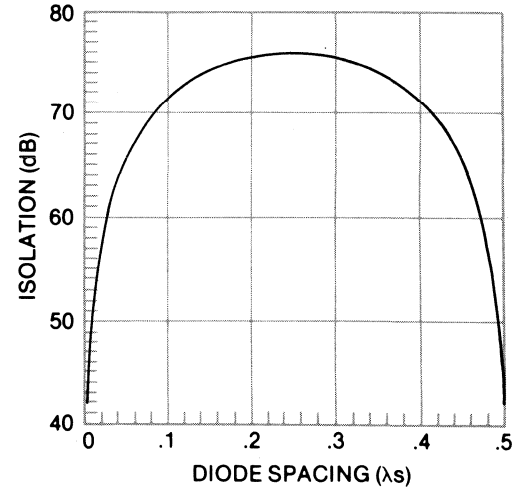


FIGURE 10.12-6 TWO SHUNT-ITERATED MA-4P505 DIODES — ISOLATION VS SPACING

PIN specification and switch performance selection guide

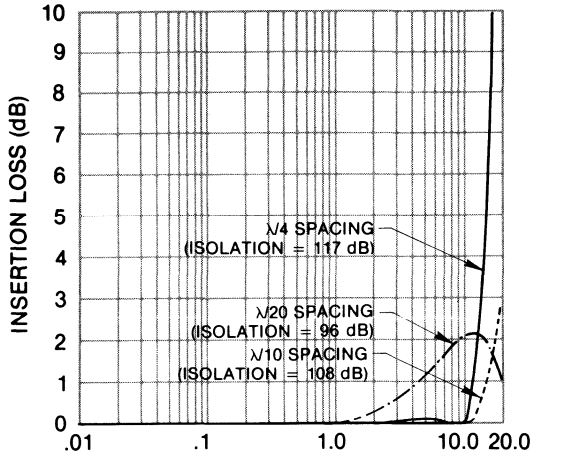


FIGURE 10.12-7 THREE SHUNT-ITERATED MA-4P505 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

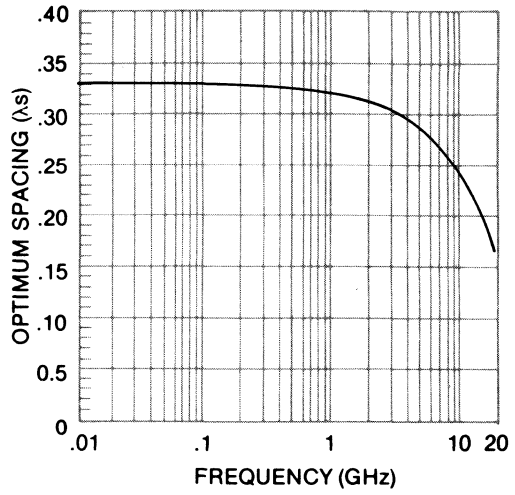


FIGURE 10.12-8 THREE SHUNT-ITERATED MA-4P505 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

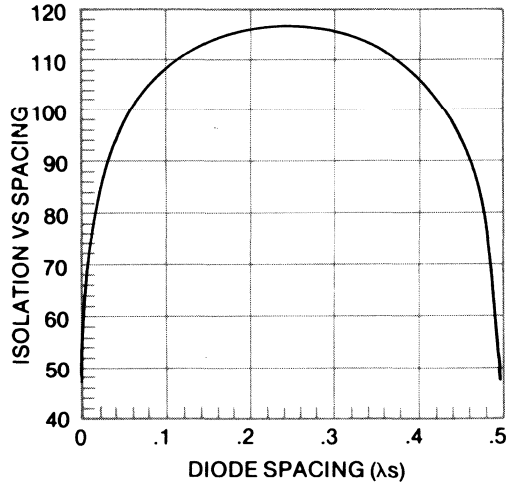


FIGURE 10.12-9 THREE SHUNT-ITERATED MA-4P505 DIODES — ISOLATION VS SPACING

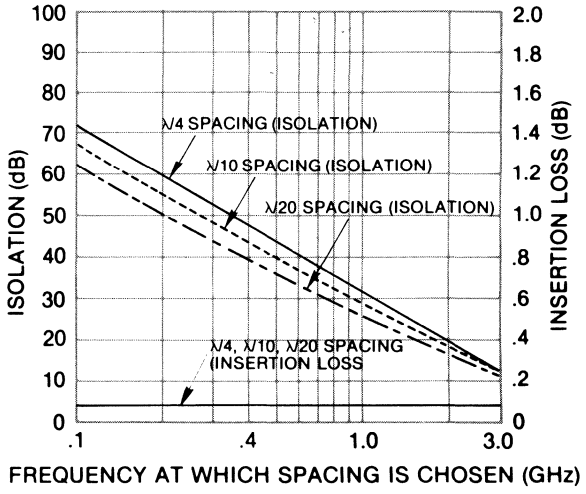


FIGURE 10.12-10 TWO SERIES-ITERATED MA-4P505 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

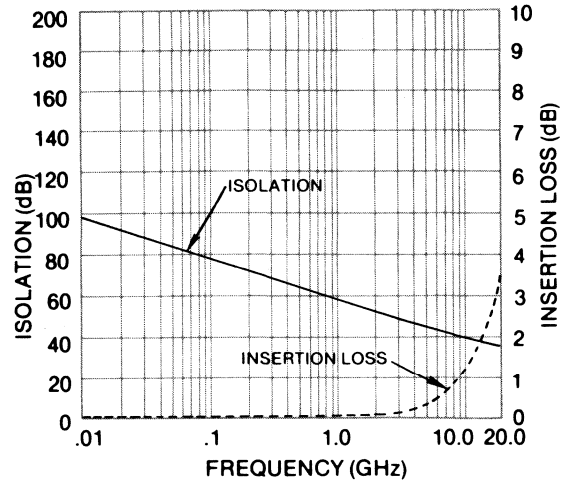


FIGURE 10.12-11 SPDT PARALLEL-SERIES MA-4P505 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

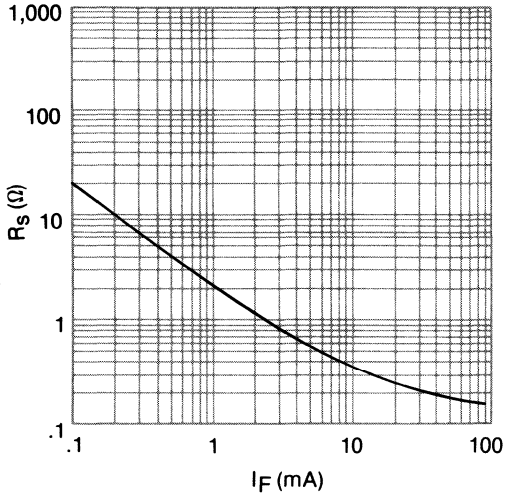
PIN specification and switch performance selection guide

10.13 MA-4P506 SPECIFICATIONS AND SWITCHING PERFORMANCE

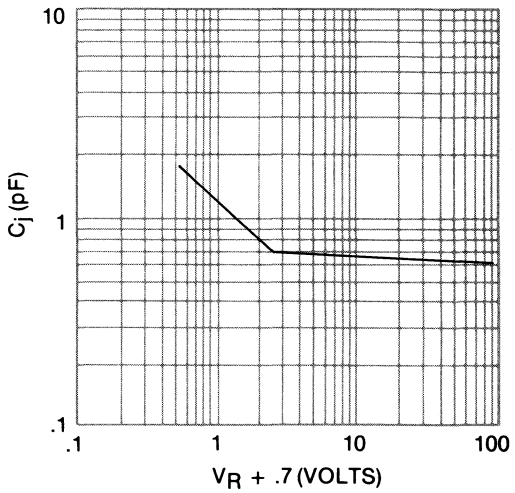
Voltage Breakdown (V_b)	=	500 volts (MIN) @ 10μA
Junction Capacitance (C_j)	=	.70 pF (MAX) @ 100 volts
Series Resistance (R_S)	=	0.3Ω (MAX) @ 100 mA
Carrier Lifetime (τ_L)	=	3.0μs (TYP)
Reverse Recovery Time (T_{rr})	=	.350 μs (TYP)
Thermal Resistance (θ_{jC})	=	10°C/W (MAX)
Power Dissipation @ 25°C	=	15W (MAX)
Standard Case Styles[1]	=	30, 4 and 131[2]

The MA-4P506 PIN diode is specifically designed for use as a moderate to high power switching diode. The low R_S, low thermal resistance and CERMACHIP™ construction of this diode make it an excellent choice for many medium power , low-loss applications. Switching speeds of 200 ns are typical.

NOTES:
1. Custom packaging is available upon request.
2. Case style 131 is a CERMACHIP™ (hermetically sealed chip).



SERIES RESISTANCE (R_S) VS FORWARD CURRENT (I_F) FOR AN MA-4P506 PIN DIODE



JUNCTION CAPACITANCE (C_j) VS REVERSE VOLTAGE (V_R) FOR AN MA-4P506 PIN DIODE

PIN specification and switch performance selection guide

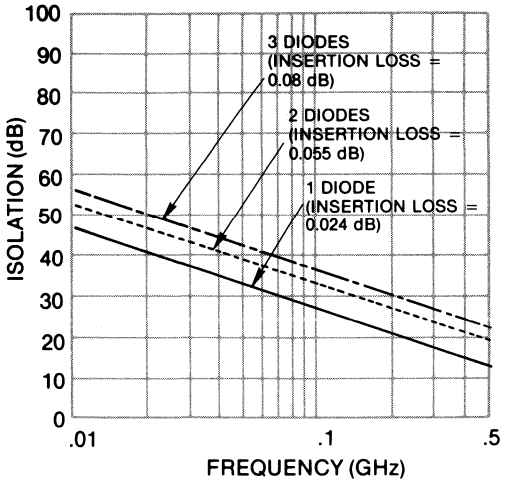


FIGURE 10.13-1 MA-4P506 SERIES DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

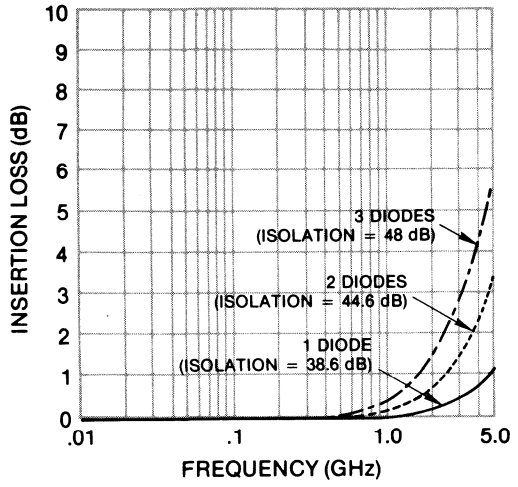


FIGURE 10.13-2 MA-4P506 SHUNT DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

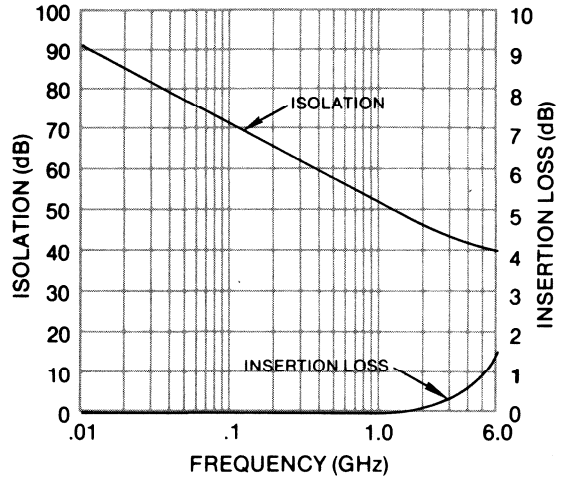


FIGURE 10.13-3 PARALLEL-SERIES MA-4P506 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

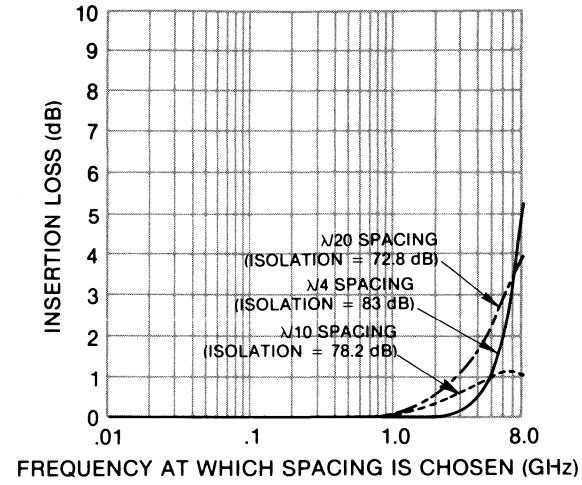


FIGURE 10.13-4 TWO SHUNT-ITERATED MA-4P506 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

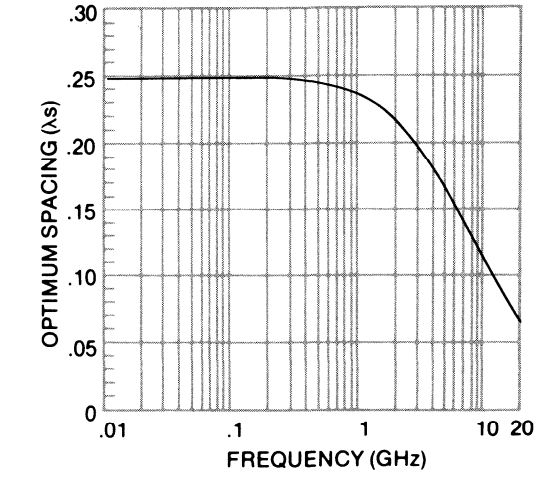


FIGURE 10.13-5 TWO SHUNT-ITERATED MA-4P506 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

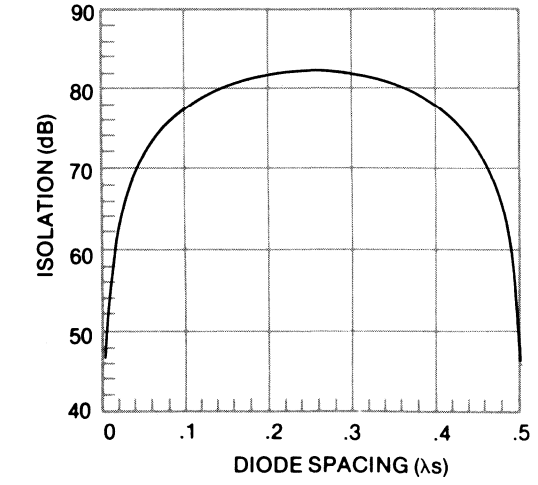


FIGURE 10.13-6 TWO SHUNT-ITERATED MA-4P506 DIODES — ISOLATION VS SPACING

PIN specification and switch performance selection guide

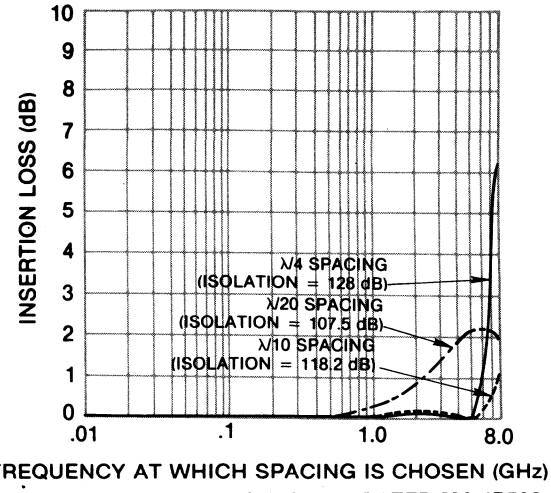


FIGURE 10.13-7 THREE SHUNT-ITERATED MA-4P506 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

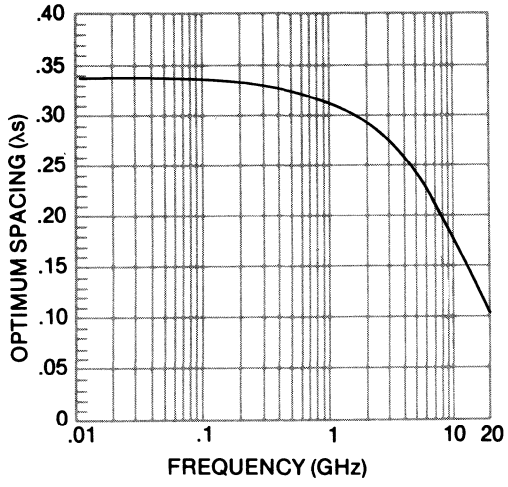


FIGURE 10.13-8 THREE SHUNT-ITERATED MA-4P506 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

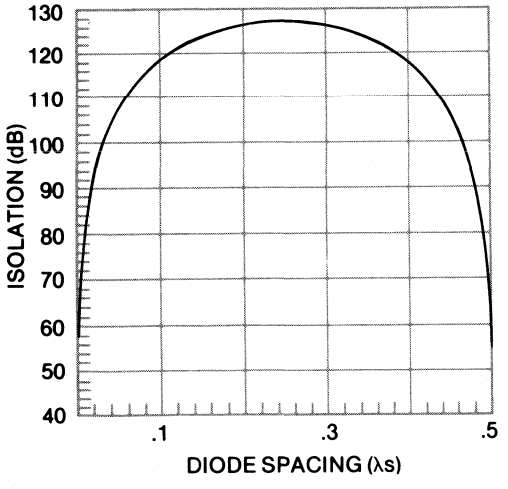


FIGURE 10.13-9 THREE SHUNT-ITERATED MA-4P506 DIODES — ISOLATION VS SPACING

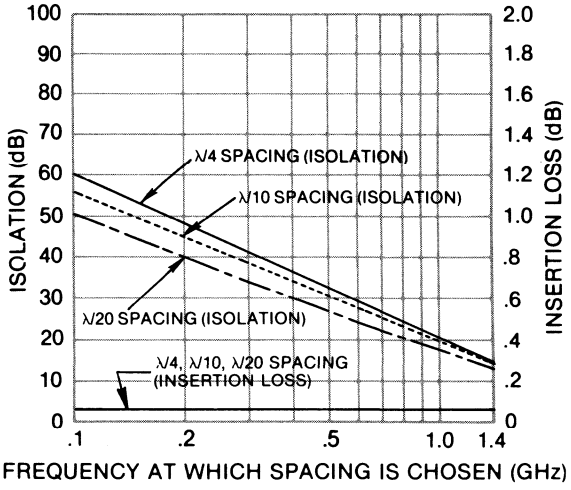


FIGURE 10.13-10 TWO SERIES-ITERATED MA-4P506 DIODES — λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

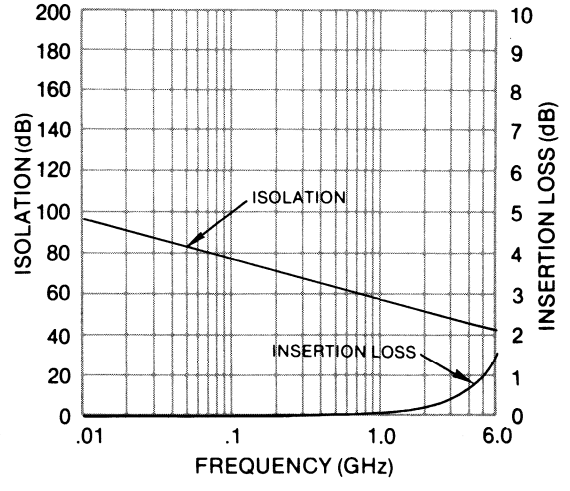


FIGURE 10.13-11 SPDT PARALLEL-SERIES MA-4P506 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

PIN specification and switch performance selection guide

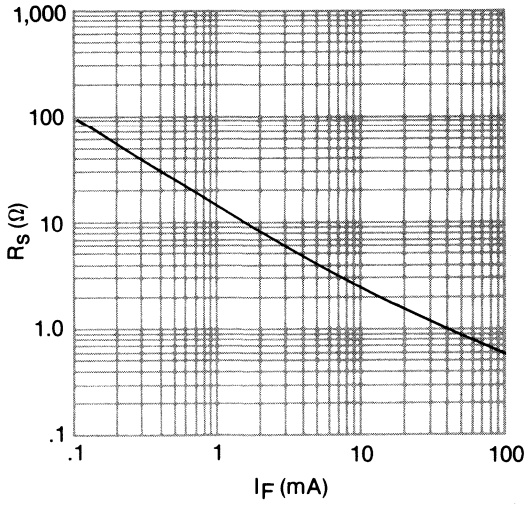
10.14 MA-4P604 SPECIFICATIONS AND SWITCHING PERFORMANCE

Voltage Breakdown (V_b)	=	1000 volts (MIN) @ 10μA
Junction Capacitance (C_j)	=	.30 pF (MAX) @ 100 volts
Series Resistance (R_S)	=	1.2Ω (MAX) @100 mA
Carrier Lifetime (τ_L)	=	3.0μs (TYP)
Reverse Recovery Time (T_{rr})	=	.700 μs (TYP)
Thermal Resistance (θ_{jC})	=	20°C/W (MAX)
Power Dissipation @ 25°C	=	7.5W (MAX)
Standard Case Styles[1]	=	30, 4 and 131[2]

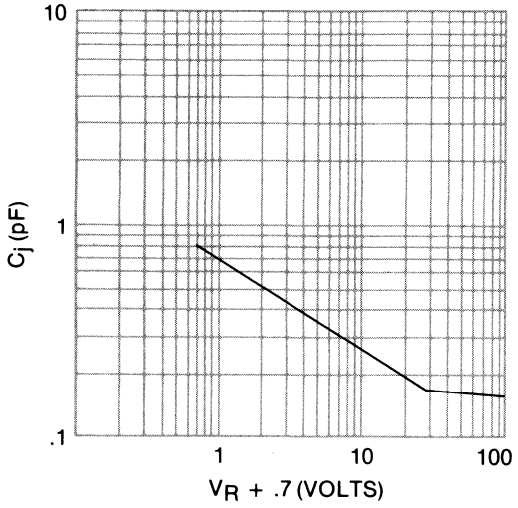
The MA-4P604 PIN diode is an excellent low-loss solution for high-power switch and phase shifter applications. Each device features CERMACHIP™ construction for maximum reliability. Typical switching time is 500 ns.

NOTES:

1. Custom packaging is available upon request.
2. Case style 131 is a CERMACHIP™ (hermetically sealed chip).



SERIES RESISTANCE (R_S) VS FORWARD CURRENT (I_F) FOR AN MA-4P604 PIN DIODE



JUNCTION CAPACITANCE (C_j) VS REVERSE VOLTAGE (V_R) FOR AN MA-4P604 PIN DIODE

PIN specification and switch performance selection guide

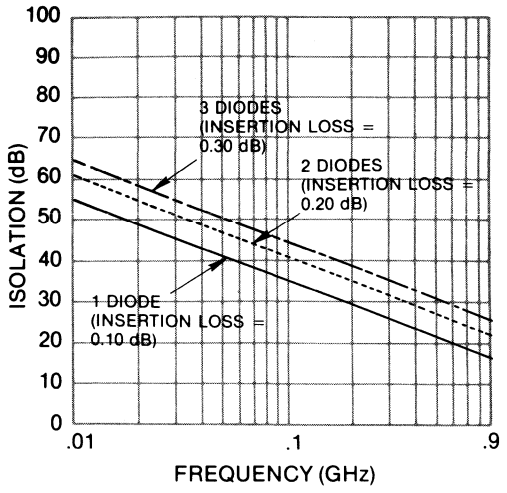


FIGURE 10.14-1 MA-4P604 SERIES DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

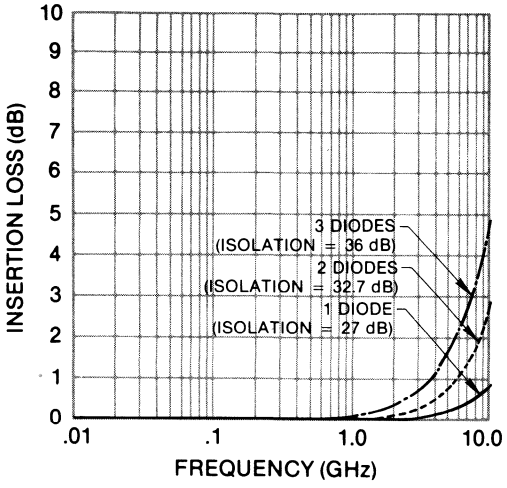


FIGURE 10.14-2 MA-4P604 SHUNT DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

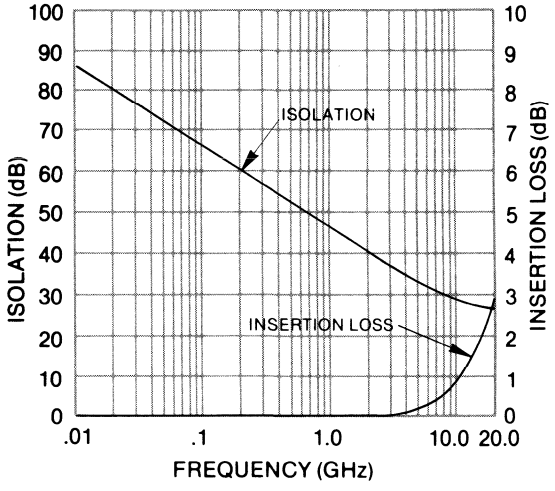


FIGURE 10.14-3 PARALLEL-SERIES MA-4P604 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

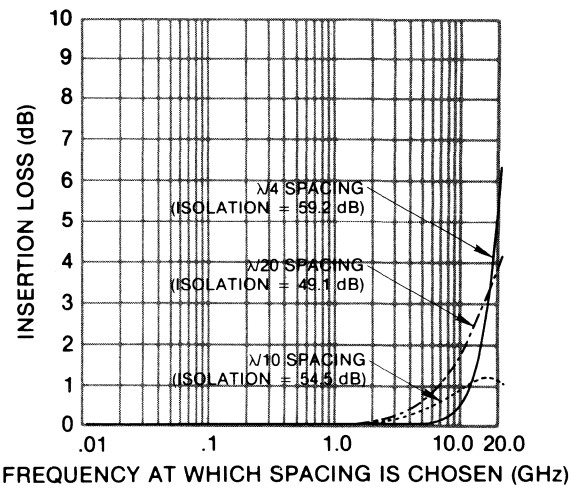


FIGURE 10.14-4 TWO SHUNT-ITERATED MA-4P604 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

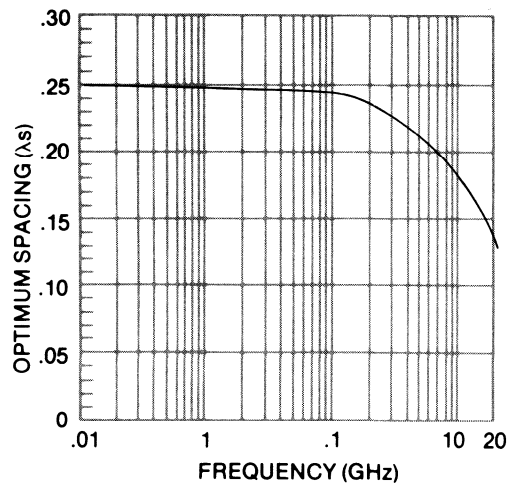


FIGURE 10.14-5 TWO SHUNT-ITERATED MA-4P604 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

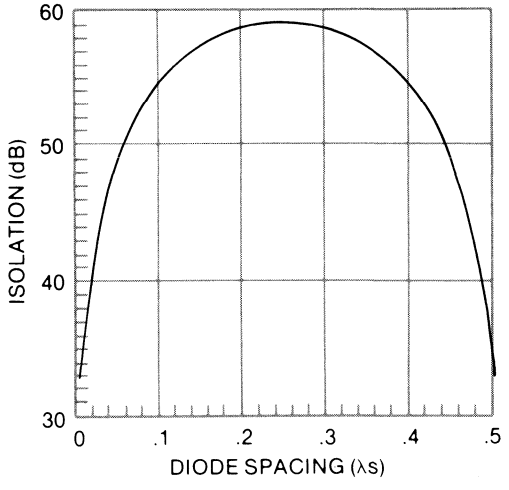


FIGURE 10.14-6 TWO SHUNT-ITERATED MA-4P604 DIODES — ISOLATION VS SPACING

PIN specification and switch performance selection guide

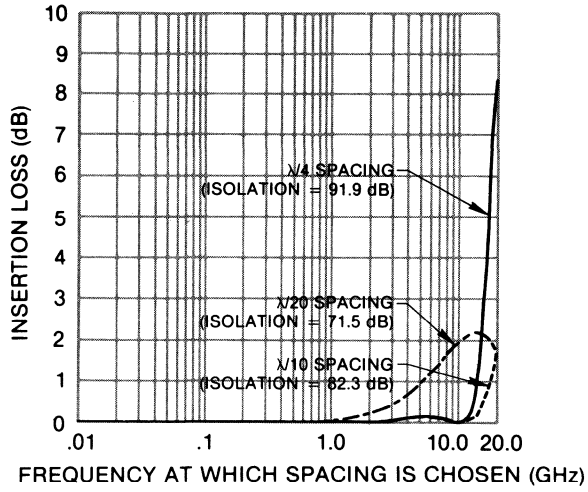


FIGURE 10.14-7 THREE SHUNT-ITERATED MA-4P604 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

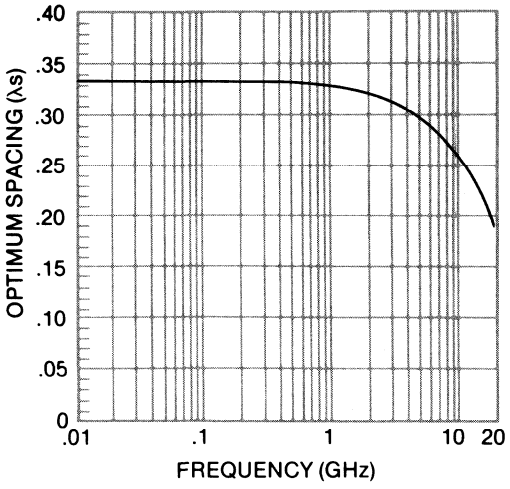


FIGURE 10.14-8 THREE SHUNT-ITERATED MA-4P604 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

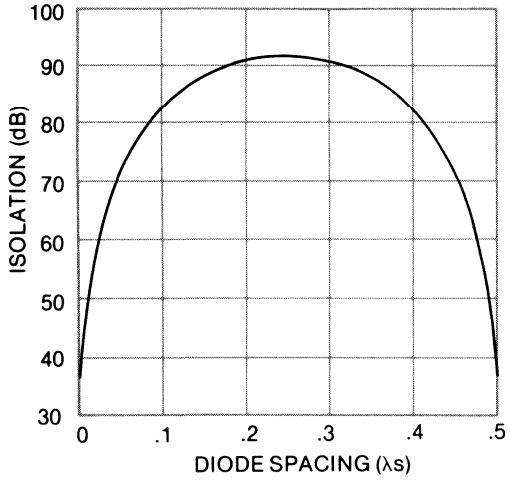


FIGURE 10.14-9 THREE SHUNT-ITERATED MA-4P604 DIODES — ISOLATION VS SPACING

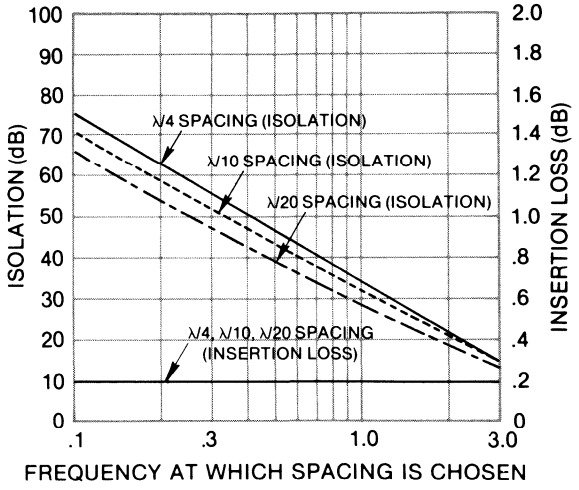


FIGURE 10.14-10 TWO SERIES-ITERATED MA-4P604 DIODES — λ/4, λ/10, λ/12 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

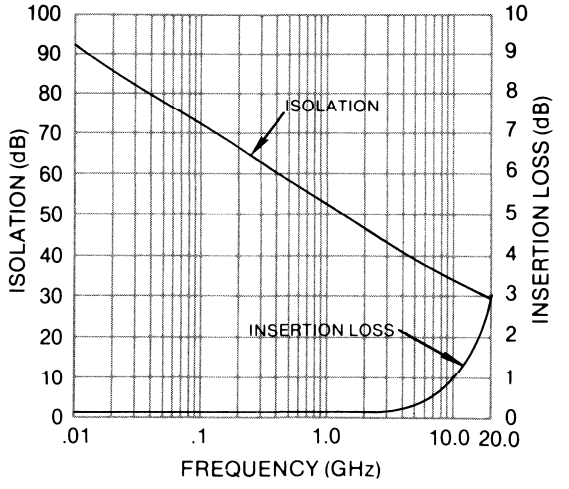


FIGURE 10.14-11 SPDT PARALLEL-SERIES MA-4P604 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

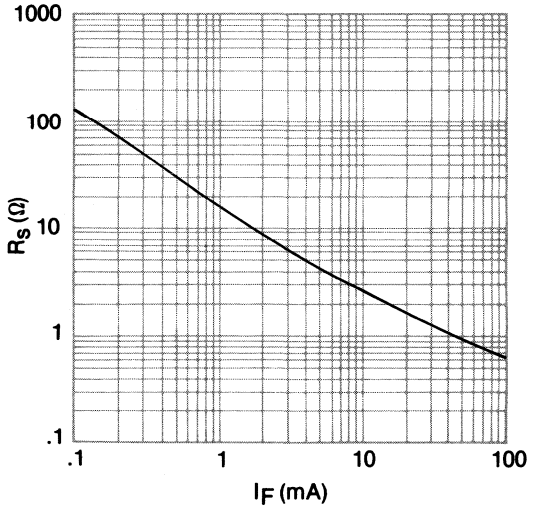
PIN specification and switch performance selection guide

10.15 MA-4P606 SPECIFICATIONS AND SWITCHING PERFORMANCE

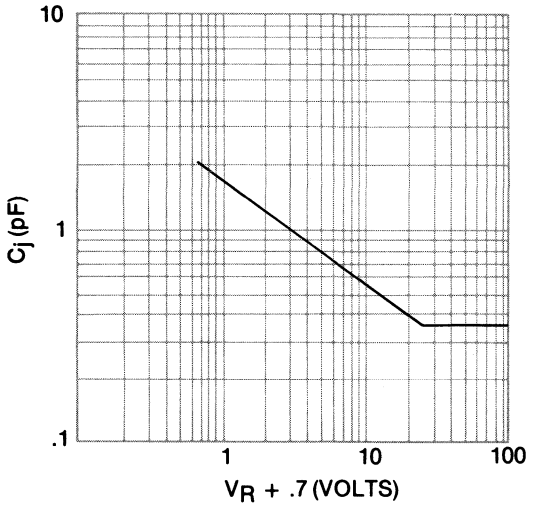
Voltage Breakdown (V_b)	=	1000 volts (MIN) @ 10μA
Junction Capacitance (C_j)	=	.60 pF (MAX) @ 100 volts
Series Resistance (R_s)	=	0.7Ω (MAX) @ 100 mA
Carrier Lifetime (τ_L)	=	4.0μs (TYP)
Reverse Recovery Time (T_{rr})	=	1.0 μs (TYP)
Thermal Resistance (θ_{jC})	=	10°C/W (MAX)
Power Dissipation @ 25°C	=	15W (MAX)
Standard Case Styles[1]	=	30, 4 and 131[2]

The MA-4P606 PIN diode is intended for use in high-power switching and phase shifting applications. Each diode features CERMACHIP™ construction, 500 ns switching time, and low thermal resistance.

NOTES:
1. Custom packaging is available upon request.
2. Case style 131 is a CERMACHIP™ (hermetically sealed chip).



SERIES RESISTANCE (R_S) VS FORWARD CURRENT (I_F) FOR AN MA-4P606 PIN DIODE



JUNCTION CAPACITANCE (C_j) VS REVERSE VOLTAGE (V_R) FOR AN MA-4P606 PIN DIODE

PIN specification and switch performance selection guide

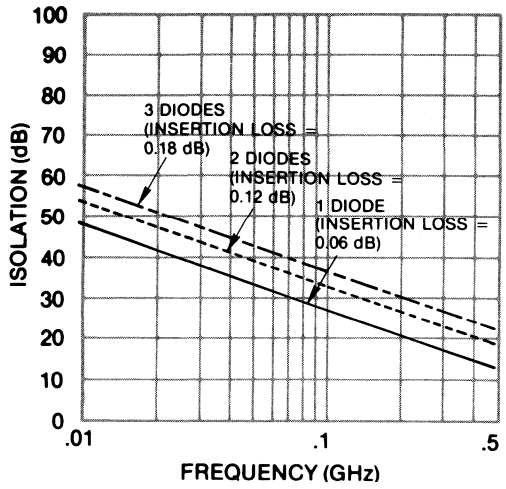


FIGURE 10.15-1 MA-4P606 SERIES DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

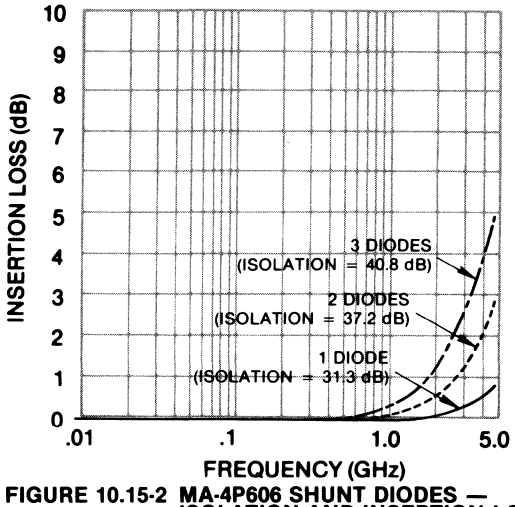


FIGURE 10.15-2 MA-4P606 SHUNT DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

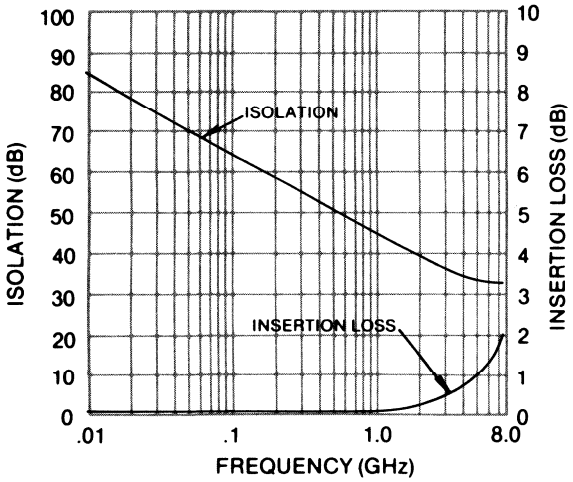


FIGURE 10.15-3 PARALLEL-SERIES MA-4P606 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

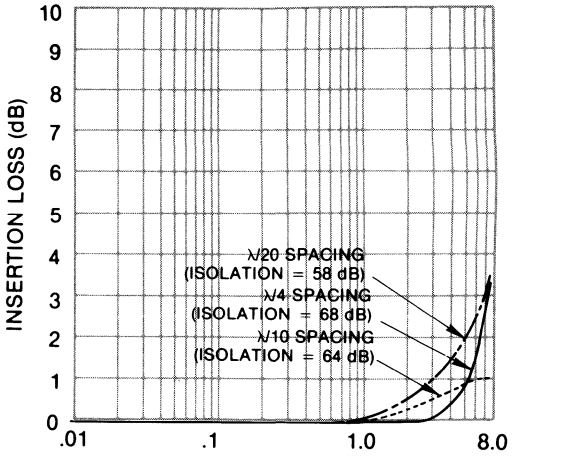


FIGURE 10.15-4 TWO SHUNT-ITERATED MA-4P608 DIODES — λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

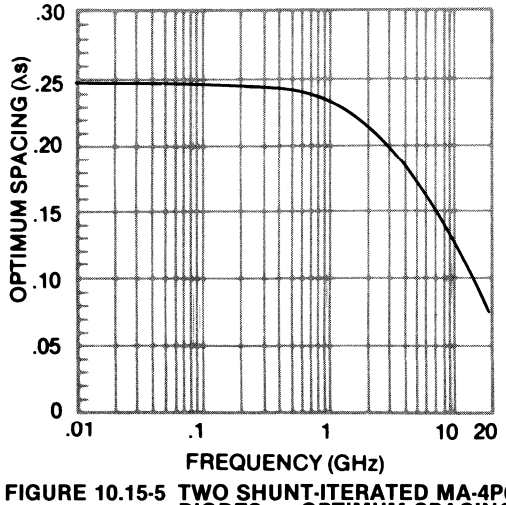


FIGURE 10.15-5 TWO SHUNT-ITERATED MA-4P606 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

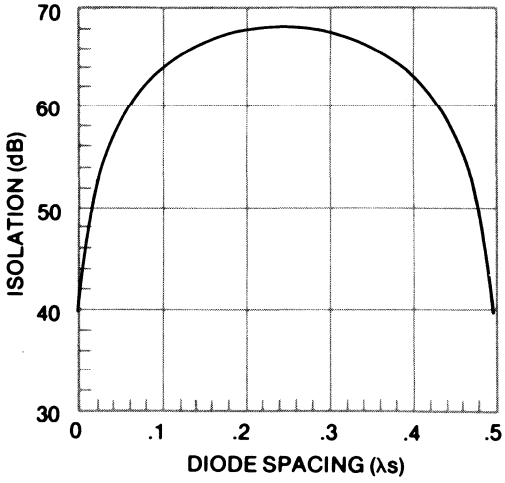


FIGURE 10.15-6 TWO SHUNT-ITERATED MA-4P606 DIODES — ISOLATION VS SPACING

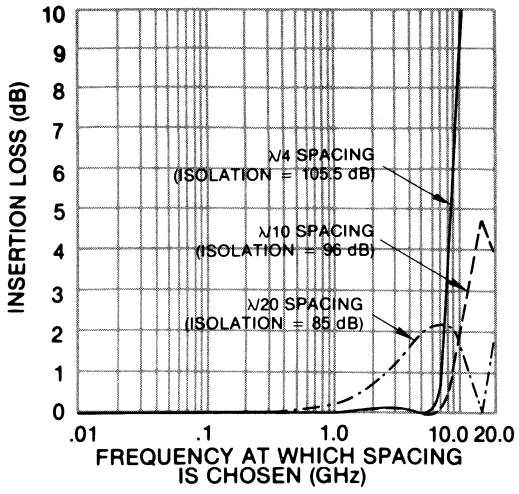


FIGURE 10.15-7 THREE SHUNT-ITERATED MA-4P606 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

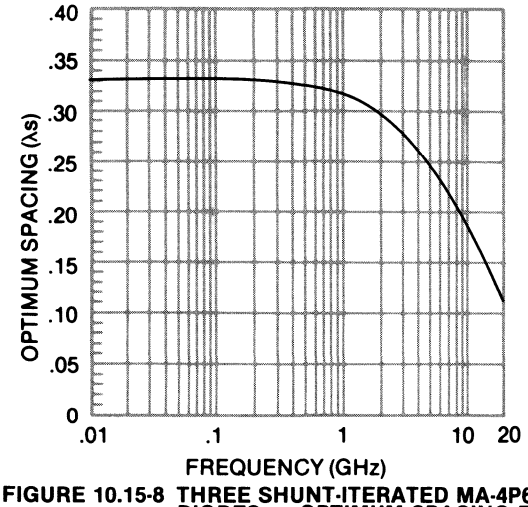


FIGURE 10.15-8 THREE SHUNT-ITERATED MA-4P606 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

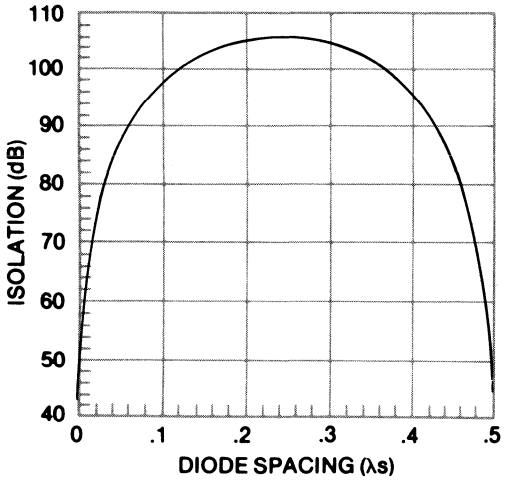


FIGURE 10.15-9 THREE SHUNT-ITERATED MA-4P606 DIODES — ISOLATION VS SPACING

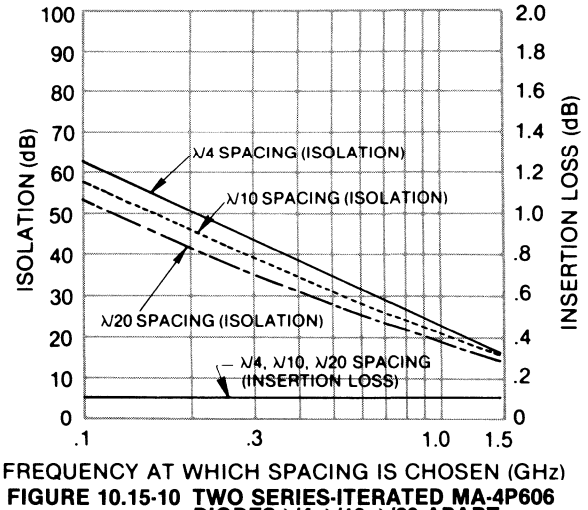


FIGURE 10.15-10 TWO SERIES-ITERATED MA-4P606 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

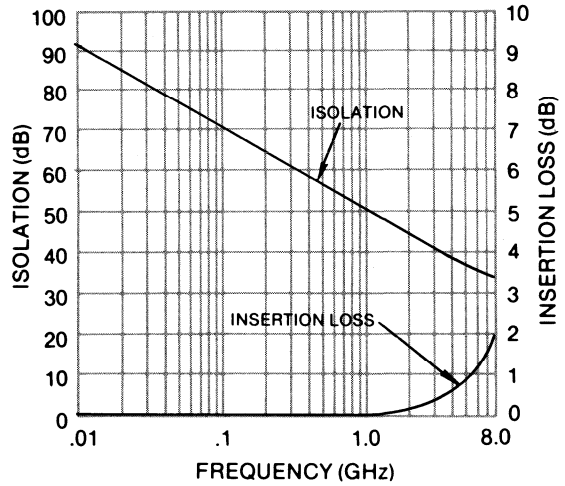


FIGURE 10.15-11 SPDT PARALLEL-SERIES MA-4P606 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

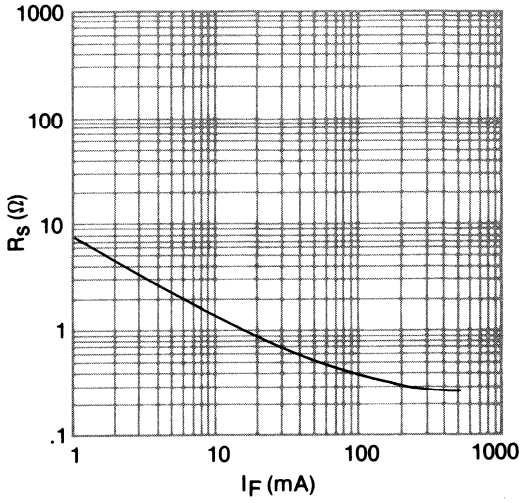
PIN specification and switch performance selection guide

10.16 MA-4P607 SPECIFICATIONS AND SWITCHING PERFORMANCE

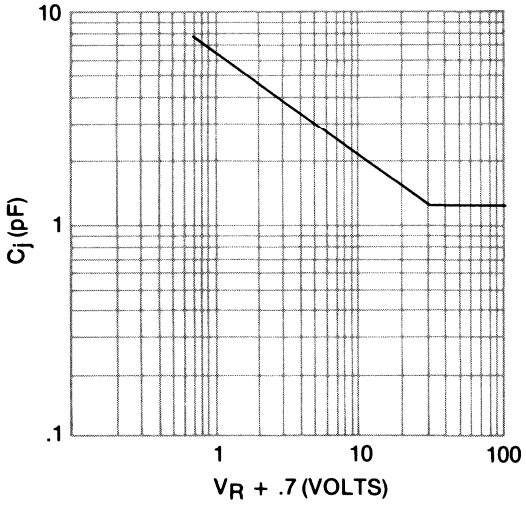
Voltage Breakdown (V_b)	=	1000 volts (MIN) @ 10μA
Junction Capacitance (C_j)	=	1.3 pF (MAX) @ 100 volts
Series Resistance (R_S)	=	0.4Ω (MAX) @ 100 mA
Carrier Lifetime (τ_L)	=	5.0μs (TYP)
Reverse Recovery Time (T_{rr})	=	1.5 μs (TYP)
Thermal Resistance (θ_{jC})	=	7°C/W (MAX)
Power Dissipation @ 25°C	=	21.4W (MAX)
Standard Case Styles[1]	=	43, 109, 150 and 212[2]

The MA-4P607 PIN diode is a lower frequency, high-power choice for both switches and phase shifters. The R_S and C_j of this diode have been optimized for minimum loss over 10% bandwidths. Switching time is typically 500 ns and CERMACHIP™ construction is used for each device.

NOTES:
1. Custom packaging is available upon request.
2. Case style 212 is a CERMACHIP™ (hermetically sealed chip).



SERIES RESISTANCE (R_S) VS FORWARD CURRENT (I_F) FOR AN MA-4P607 PIN DIODE



JUNCTION CAPACITANCE (C_j) VS REVERSE VOLTAGE (V_R) FOR AN MA-4P607 PIN DIODE

PIN specification and switch performance selection guide

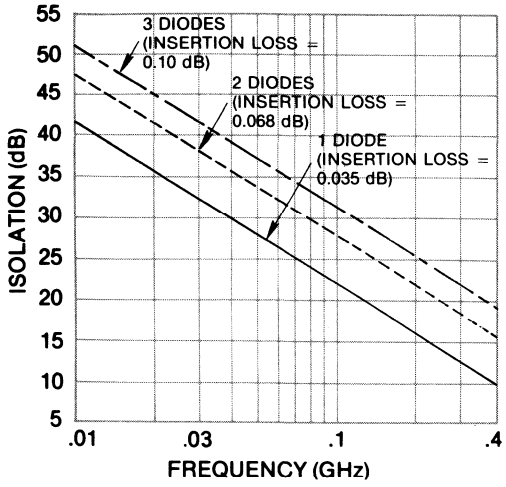


FIGURE 10.16-1 MA-4P607 SERIES DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

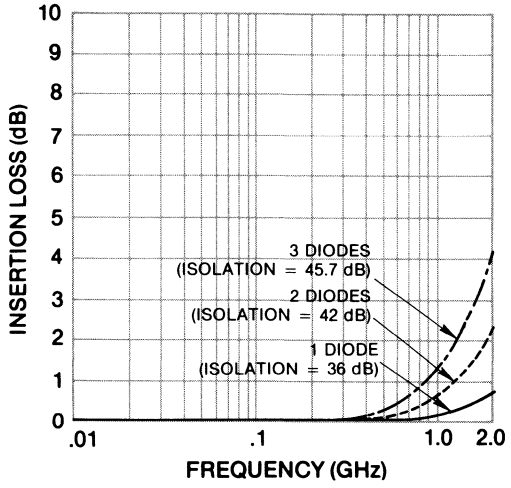


FIGURE 10.16-2 MA-4P607 SHUNT DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

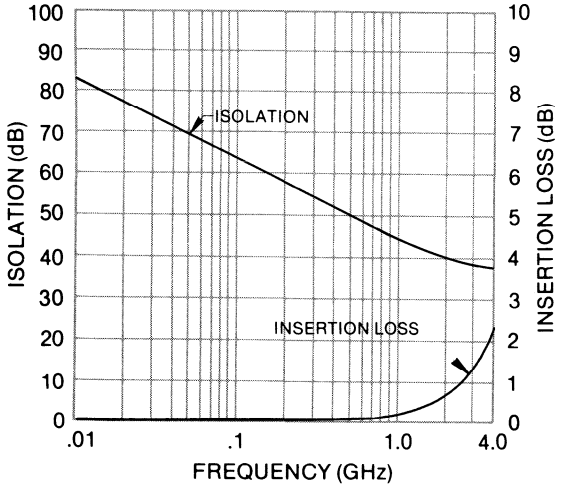


FIGURE 10.16-3 PARALLEL-SERIES MA-4P607 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

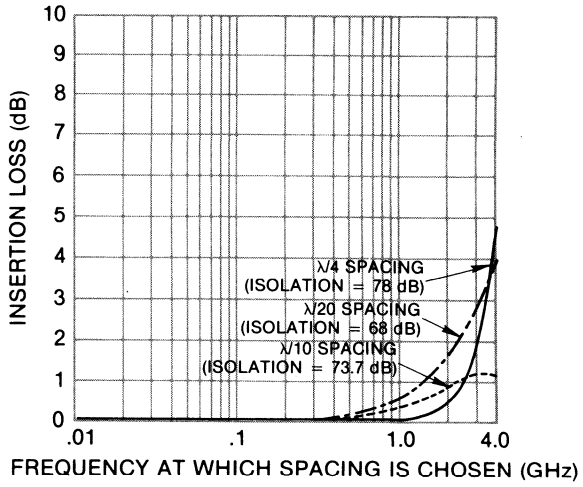


FIGURE 10.16-4 TWO SHUNT-ITERATED MA-4P607 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

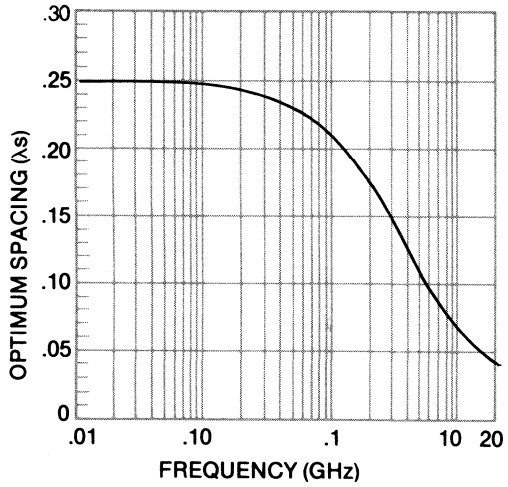


FIGURE 10.16-5 TWO SHUNT-ITERATED MA-4P607 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

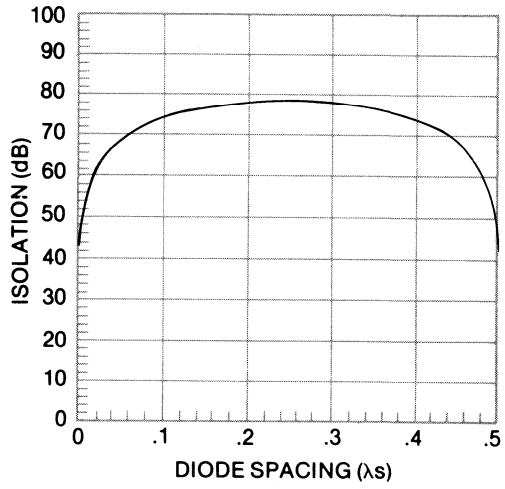


FIGURE 10.16-6 TWO ITERATED MA-4P607 SHUNT DIODES — ISOLATION VS SPACING

PIN specification and switch performance selection guide

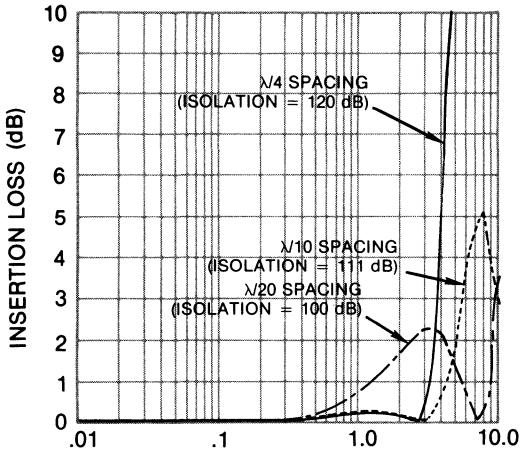


FIGURE 10.16-7 THREE SHUNT-ITERATED MA-4P607 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

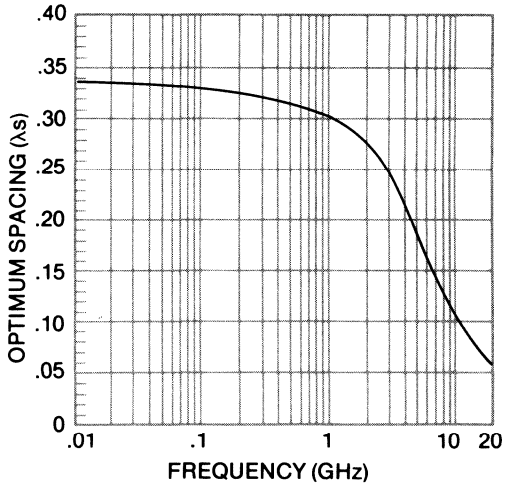


FIGURE 10.16-8 THREE SHUNT-ITERATED MA-4P607 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

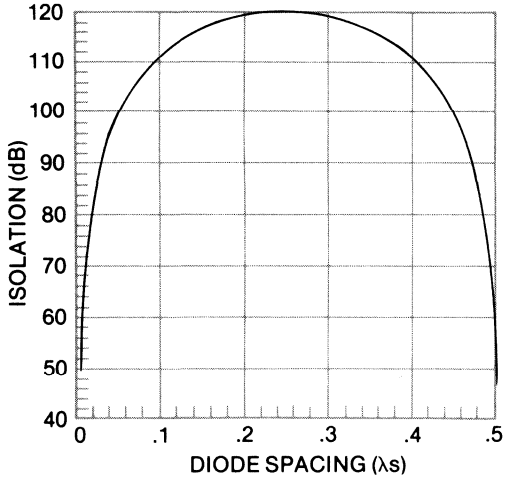


FIGURE 10.16-9 THREE SHUNT-ITERATED MA-4P607 DIODES — ISOLATION VS SPACING

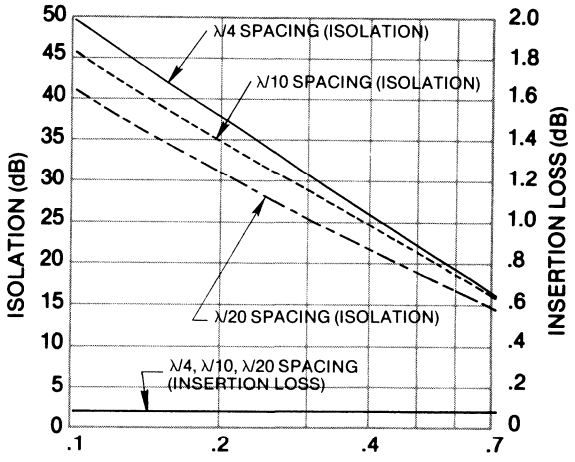


FIGURE 10.16-10 TWO SERIES-ITERATED MA-4P607 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

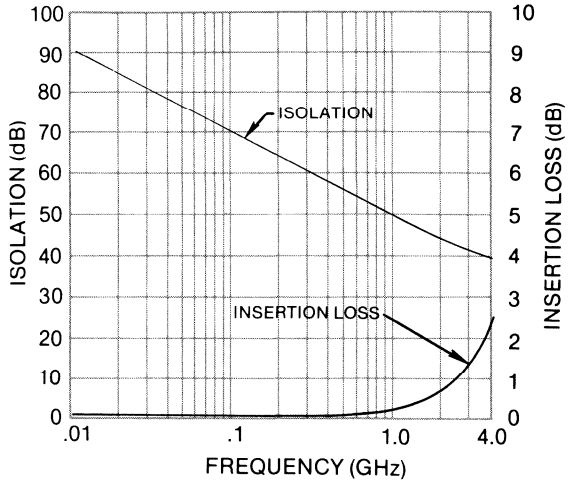


FIGURE 10.16-11 SPDT PARALLEL-SERIES MA-4P607 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

PIN specification and switch performance selection guide

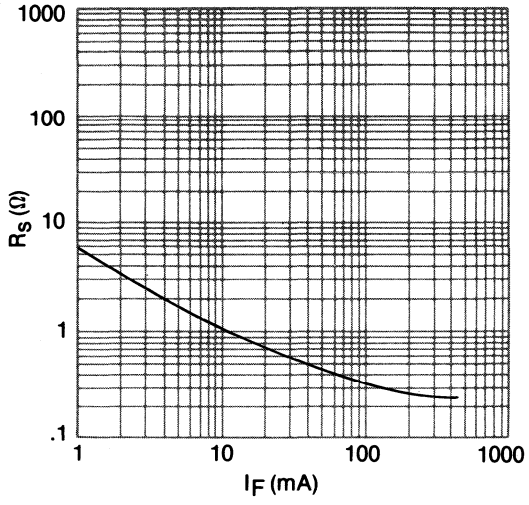
10.17 MA-4P608 SPECIFICATIONS AND SWITCHING PERFORMANCE

Voltage Breakdown (V_b)	=	1000 volts (MIN) @ 10μA
Junction Capacitance (C_j)	=	2.5 pF (MAX) @ 100 volts
Series Resistance (R_S)	=	.35Ω (MAX) @ 100 mA
Carrier Lifetime (τ_L)	=	5.0μs (TYP)
Reverse Recovery Time (T_{rr})	=	1.5 μs (TYP)
Thermal Resistance (θ_{jC})	=	5°C/W (MAX)
Power Dissipation @ 25°C	=	30W (MAX)
Standard Case Styles[1]	=	43, 109, 130[2] and 150

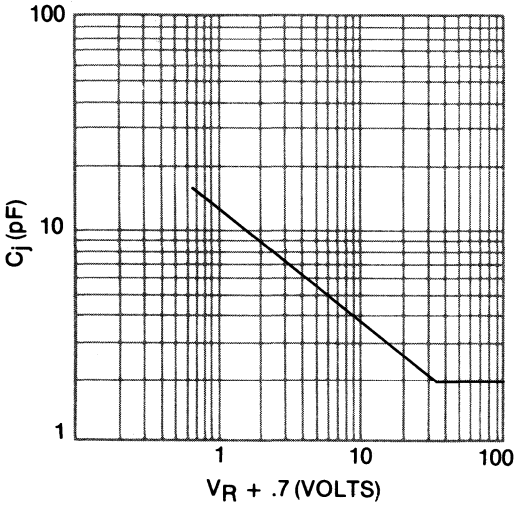
CERMACHIP™ construction and moderate values of junction capacitance make the MA-4P608 PIN diode the highest power solution for switching and phase shifter applications in the MA-4P600 family. This device is designed for low frequency operation over bandwidths of 10% or less. Switching time is typically 500 ns.

NOTES:

1. Custom packaging is available upon request.
2. Case style 130 is a CERMACHIP™ (hermetically sealed chip).



SERIES RESISTANCE (R_S) VS FORWARD CURRENT (I_F) FOR AN MA-4P608 PIN DIODE



JUNCTION CAPACITANCE (C_j) VS REVERSE VOLTAGE (V_R) FOR AN MA-4P608 PIN DIODE

PIN specification and switch performance selection guide

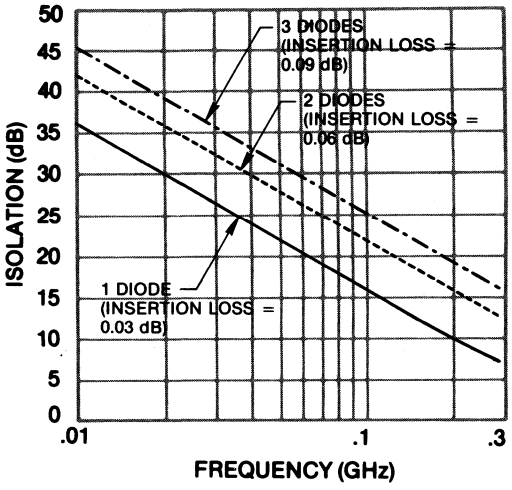


FIGURE 10.17-1 MA-4P608 SERIES DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

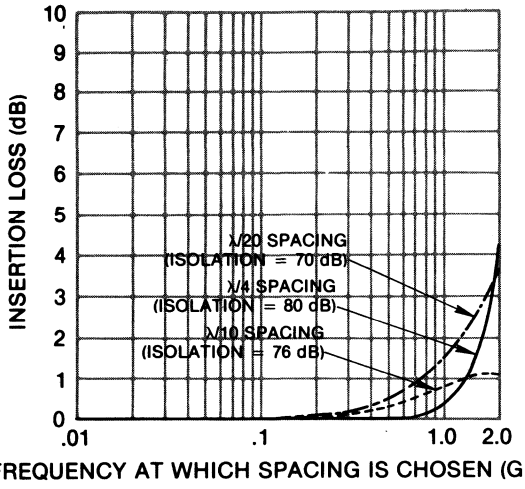


FIGURE 10.17-4 TWO SHUNT-ITERATED MA-4P608 DIODES — λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

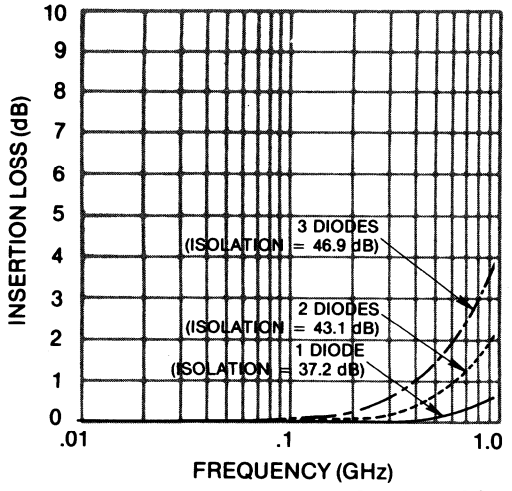


FIGURE 10.17-2 MA-4P608 SHUNT DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

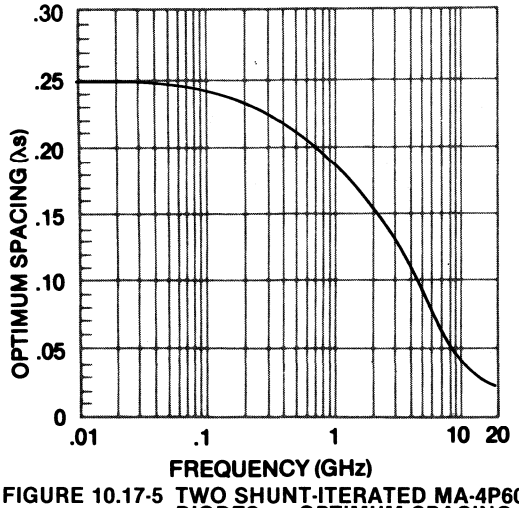


FIGURE 10.17-5 TWO SHUNT-ITERATED MA-4P608 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

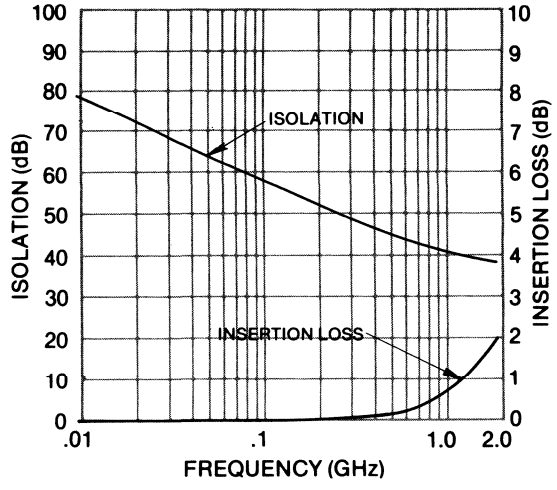


FIGURE 10.17-3 PARALLEL-SERIES MA-4P608 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

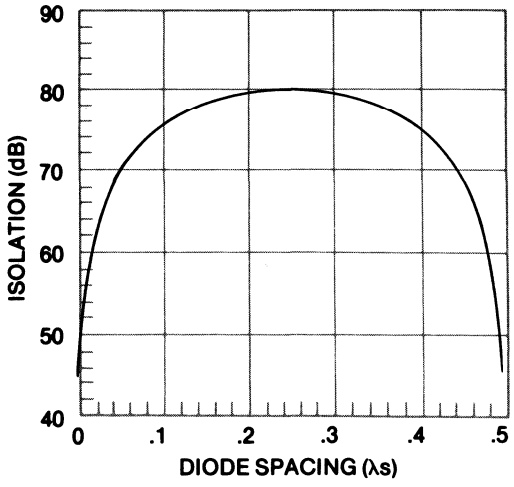


FIGURE 10.17-6 TWO SHUNT-ITERATED MA-4P608 DIODES — ISOLATION VS SPACING

PIN specification and switch performance selection guide

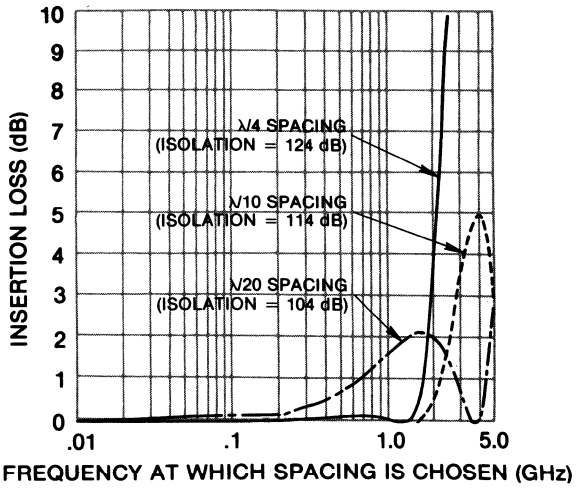


FIGURE 10.17-7 THREE SHUNT-ITERATED MA-4P608 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

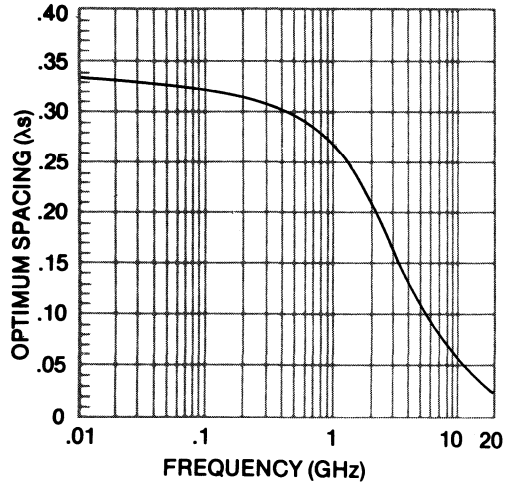


FIGURE 10.17-8 THREE SHUNT-ITERATED MA-4P608 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

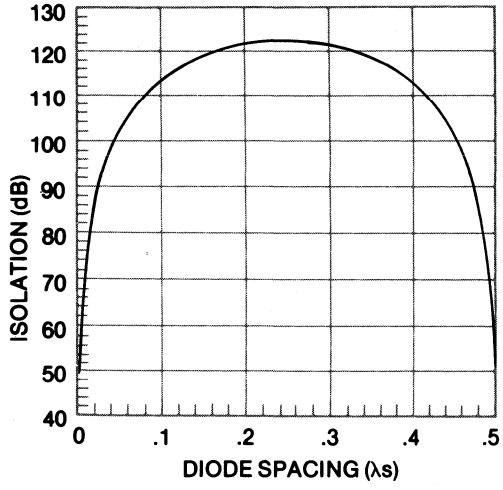


FIGURE 10.17-9 THREE SHUNT-ITERATED MA-4P608 DIODES — ISOLATION VS SPACING

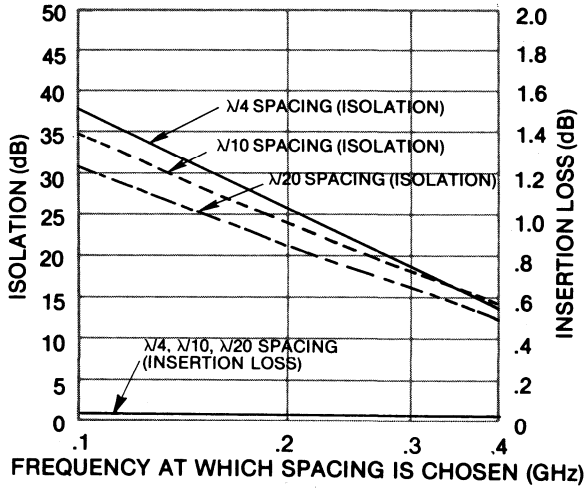


FIGURE 10.17-10 TWO SERIES-ITERATED MA-4P608 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

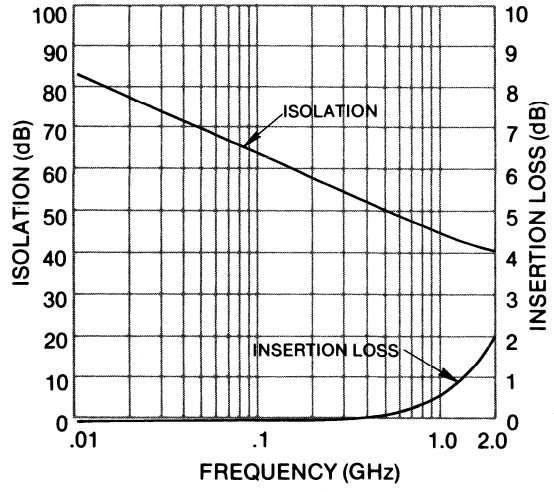


FIGURE 10.17-11 SPDT PARALLEL-SERIES MA-4P608 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

PIN specification and switch performance selection guide

140

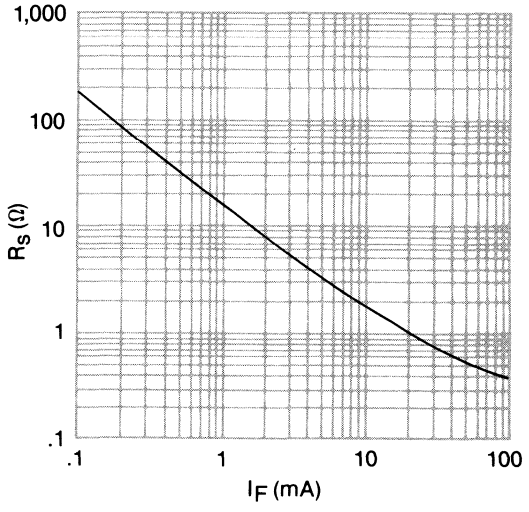
10.18 MA-4P709 SPECIFICATIONS AND SWITCHING PERFORMANCE

Voltage Breakdown (V_b)	=	1500 volts (MIN) @ 10μA
Junction Capacitance (C_j)	=	3.3 pF (MAX) @ 100 volts
Series Resistance (R_s)	=	0.35Ω (MAX) @ 200 mA
Carrier Lifetime (τ_L)	=	8μs (TYP)
Reverse Recovery Time (T_{rr})	=	2 μs (TYP)
Thermal Resistance (θ_{jc})	=	2°C/W (MAX)
Power Dissipation @ 25°C	=	75W (MAX)
Standard Case Styles[1]	=	150 and 223[2]

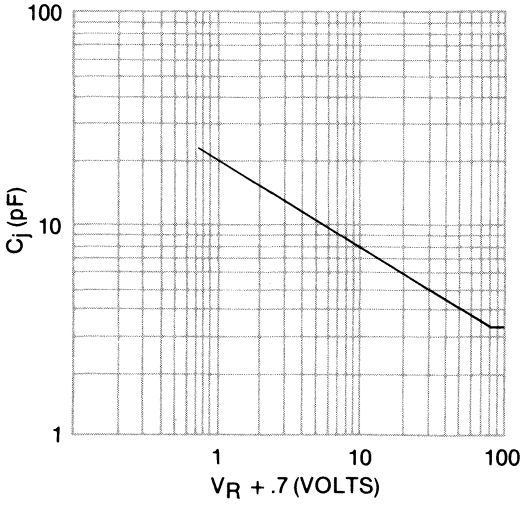
The MA-4P709 CERMACHIP™ PIN diode is designed to handle the highest power of all the MA-4P standard family of PIN diodes. Typical applications include low frequency, narrow band switches and phase shifters. The switching time of this device is typically 1μs.

NOTES:

1. Custom packaging is available upon request.
2. Case style 223 is a CERMACHIP™ (hermetically sealed chip).



SERIES RESISTANCE (R_s) VS FORWARD CURRENT (I_F) FOR AN MA-4P709 PIN DIODE



JUNCTION CAPACITANCE (C_j) VS REVERSE VOLTAGE (V_R) FOR AN MA-4P709 PIN DIODE

PIN specification and switch performance selection guide

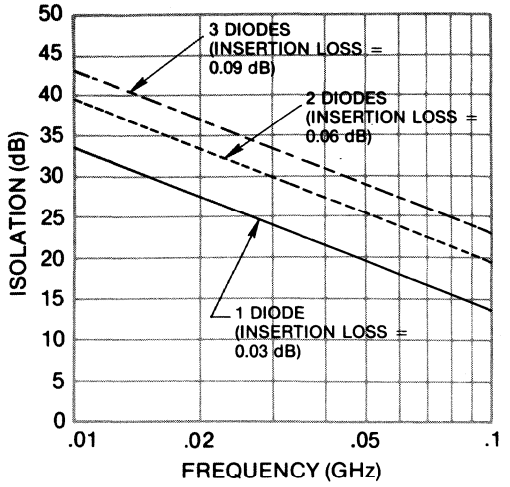


FIGURE 10.18-1 MA-4P709 SERIES DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

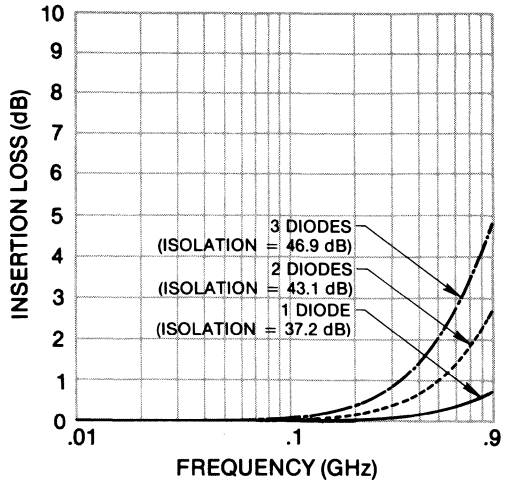


FIGURE 10.18-2 MA-4P709 SHUNT DIODES — ISOLATION AND INSERTION LOSS VS FREQUENCY

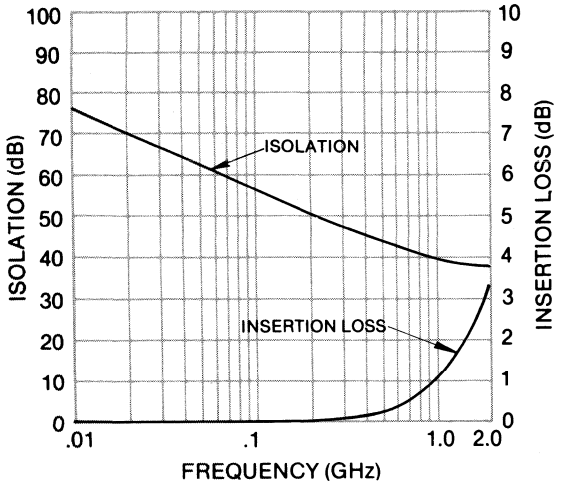


FIGURE 10.18-3 PARALLEL-SERIES MA-4P709 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

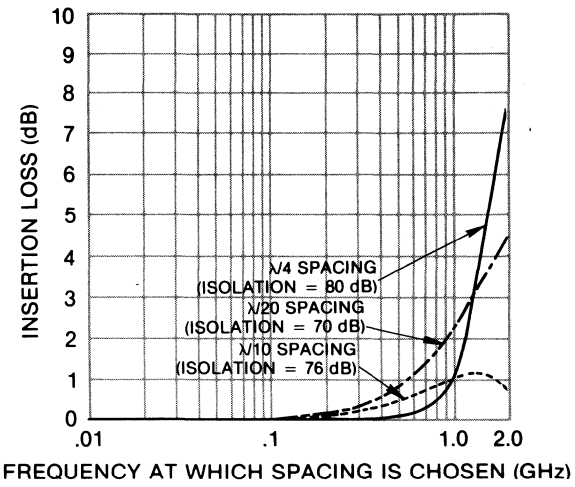


FIGURE 10.18-4 TWO SHUNT-ITERATED MA-4P709 DIODES — λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

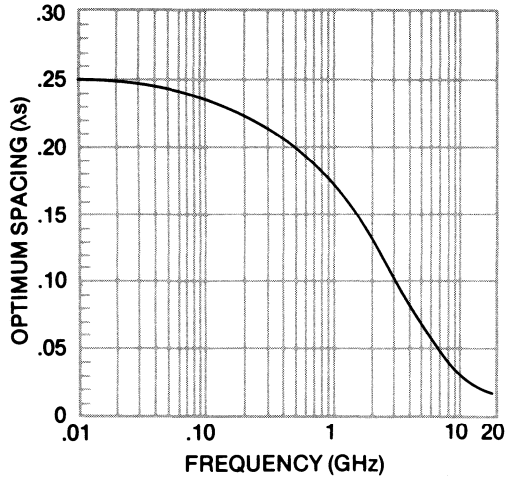


FIGURE 10.18-5 TWO SHUNT-ITERATED MA-4P709 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

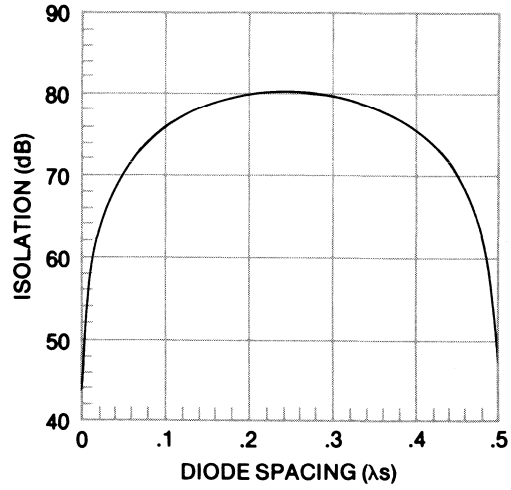


FIGURE 10.18-6 TWO SHUNT-ITERATED MA-4P709 DIODES — ISOLATION VS SPACING

PIN specification and switch performance selection guide

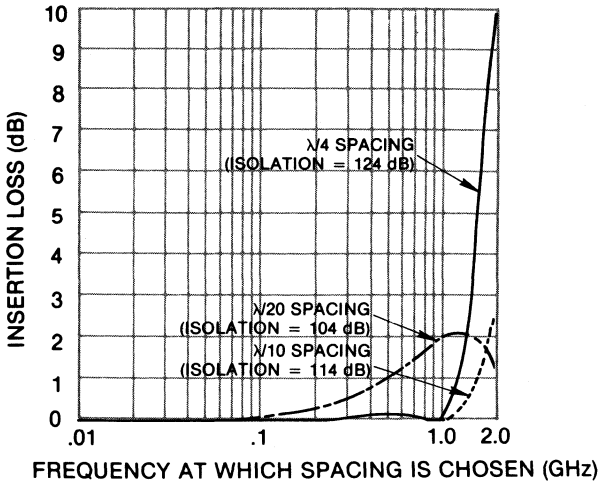


FIGURE 10.18-7 THREE SHUNT-ITERATED MA-4P709 DIODES — λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

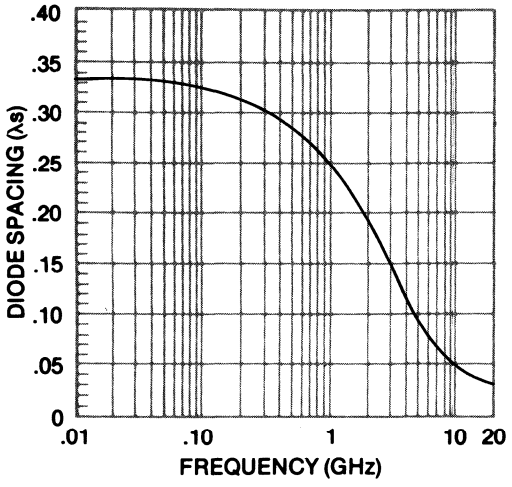


FIGURE 10.18-8 THREE SHUNT-ITERATED MA-4P709 DIODES — OPTIMUM SPACING FOR MINIMUM INSERTION LOSS AS A FUNCTION OF FREQUENCY

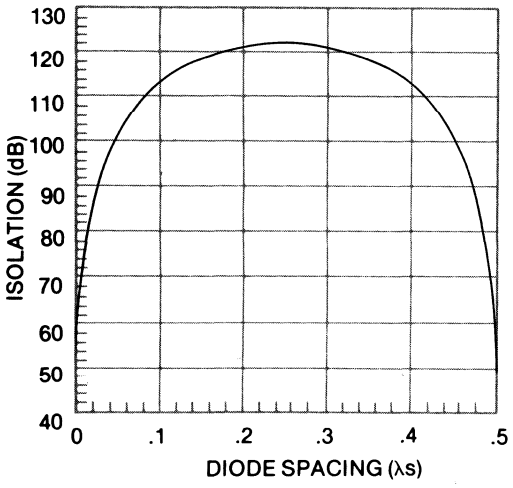


FIGURE 10.18-9 THREE SHUNT-ITERATED MA-4P709 DIODES — ISOLATION VS SPACING

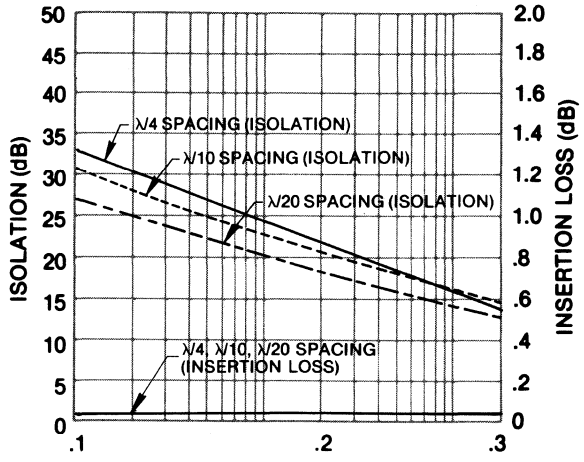


FIGURE 10.18-10 TWO SERIES-ITERATED MA-4P709 DIODES λ/4, λ/10, λ/20 APART — ISOLATION AND INSERTION LOSS VS FREQUENCY

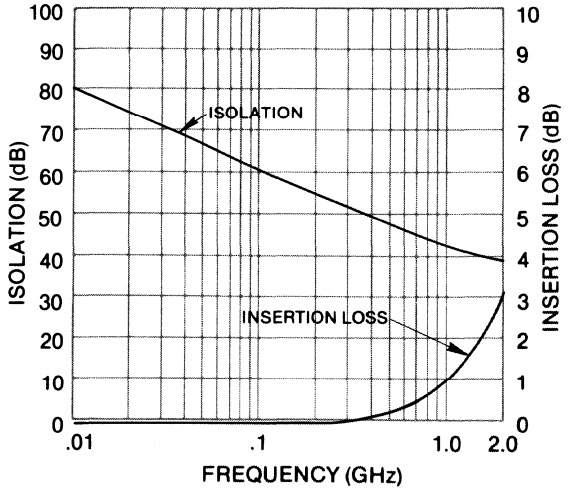


FIGURE 10.18-11 SPDT PARALLEL-SERIES MA-4P709 DIODE SWITCH — ISOLATION AND INSERTION LOSS VS FREQUENCY

product overview

11.1 DISCUSSION

Microwave Associates PIN diodes are presented in a new, comprehensive diode matrix selection guide, that allows simple selection of PIN diodes as a function of breakdown voltage and junction capacitance for virtually every RF and microwave circuit application.

This matrix features diodes produced by the most modern processing techniques in the semiconductor industry today. Each diode type has optimally tailored junction profiles and gold metallization. Many of the diode types feature our hermetically sealed chip passivation, CERMACHIP™. Implicit in our processing techniques is diode uniformity and quality. The diodes are available in chip form and in a variety of packages suitable for use in any circuit medium; both are capable of meeting the most stringent environmental reliability tests and can be ordered with testing to any selected reliability level.

11.2 APPLICATIONS

These diodes are designed for use in low, medium and high power RF switches, phase shifters, duplexers, modulators and attenuators. The chip diodes are particularly well suited for mounting in microwave integrated circuits and modules.

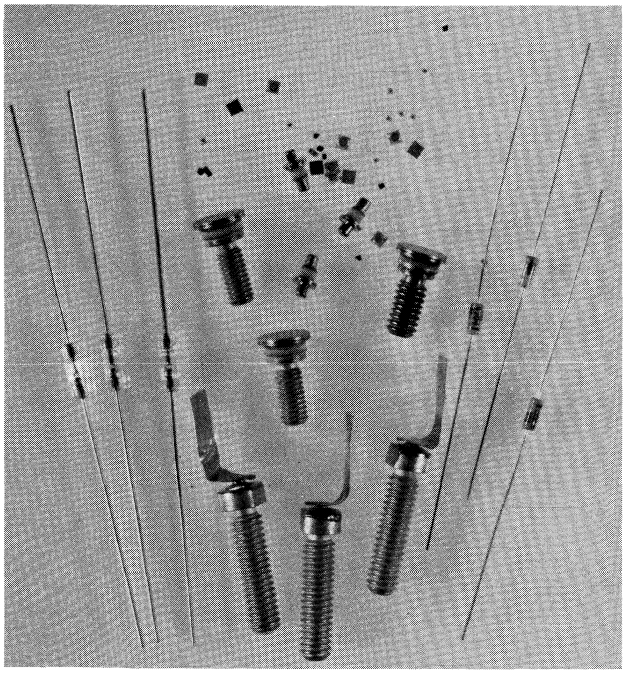


FIGURE 11.3-1 PIN DIODE CASE STYLE SELECTION

11.3 FEATURES

- HERMETICALLY SEALED CHIPS
- V_B FROM 40 TO 1500 VOLTS
- C_j VALUES FROM .02 To 3 pF
- θ_{jc} AS LOW AS 3°C/WATT
- R_S AS LOW AS 0.3 OHMS
- OFF THE SHELF AVAILABILITY
- ULTRA HIGH RELIABILITY FOR SPACE/ MILITARY APPLICATIONS
- LOW COST

11.4 DIODE SELECTION

The selection of a PIN diode for a specific application is often made unnecessarily complex. In the past, diode manufacturer's data often gave little of the information needed for use in PIN diode design equations. Microwave Associates' line of standard PIN diodes has been organized to reverse this trend and simplify the choice of diodes for specific applications.

The major characteristics of a PIN diode are its breakdown voltage V_B, and its capacitance, C_T. The breakdown voltage is an indication of the intrinsic layer width and relates directly to power handling and switching speed properties. The capacitance, C_T, is measured at a reverse voltage greater than punch through, where the diode capacitance is minimum and represents the capacitance measured at RF frequencies. C_T is the sum of junction capacitance, C_j, and case capacitance, C_P. When unpackaged chips are used, C_T is equal to C_j. C_j relates to power handling via junction size and to electrical impedance via the PIN diode model which represents the diode as a capacitor with value C_j in the reverse bias state.

Figures 11.4-1 through 11.4-4 are design aids for you to select the PIN diode best suited for your application. These figures are to be used in the following way:

The selection process starts with Figure 11.4-1 which lists PIN diode breakdown voltage, V_B, versus application. Thus the application determines the V_B parameter. The user then proceeds to Figure 11.4-2 which displays recommended junction capacitance, C_j, versus operation, frequency and bandwidth. The operation, frequency and intended bandwidth thus determine the desired C_j value. Having determined V_B and C_j the user enters the standard pin diode matrix of Figure 11.4-3 to determine the exact model PIN diode appropriate for his application. In this manner, the diode chip is determined. Figure 11.4-4 lists the standard package styles available for each

standard chip. A complete designation of a standard PIN diode consists of the chip number with a package number suffix. For example, a model MA-4P303 chip in a miniature axial glass package would be designated as MA-4P303-54.

	VOLTAGE BREAKDOWN
LIMITERS	
TO 200 WATTS	30
TO 1 kW	100
FAST SWITCHING	
4 NANOSECONDS	30
20	100
50	200
100	300
200	500
500	1000
1 MICROSECOND	1500
GENERAL PURPOSE SWITCHING & PHASE SHIFTING	100 - 500
HIGH POWER SWITCHING & PHASE SHIFTING	500 - 1500

FIGURE 11.4-1 PIN FUNCTIONS BY VOLTAGE BREAKDOWN

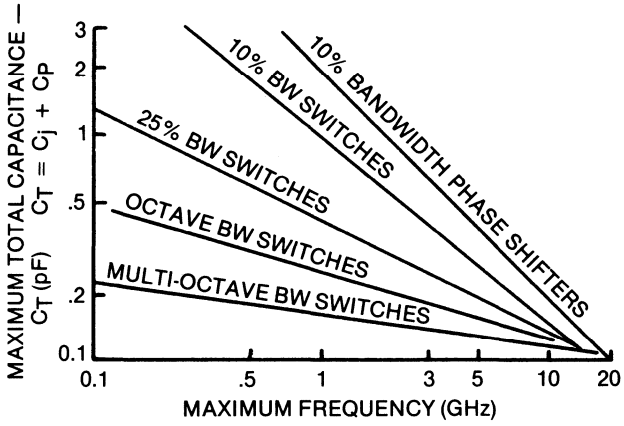


FIGURE 11.4-2 SELECTING PIN DIODE CAPACITANCE BASED ON CIRCUIT BANDWIDTH AND MAXIMUM FREQUENCY

Nominal Junction Capacitance[1] — C_j (pF)	Nominal Breakdown Voltage[2] — V_B (Volts)						
	30	100	200	300	500	1000	1500
.02	MA-4P101[3]						
.05	MA-4P102[4]	MA-4P202					
.15	MA-4P103	MA-4P203	MA-4P303				
.2				MA-4P404	MA-4P504	MA-4P604	
.3					MA-4P505		
.5					MA-4P506	MA-4P606	
1.0						MA-4P607	
2.0						MA-4P608	
3.0							MA-4P709

NOTES:
1. f = 1 MHz, V_R = 10 to 100 volts dc, depending on model number.
2. Breakdown voltage is measured at a reverse current (I_R) of 10μA dc.
3. The MA-4P101 is a beam lead device.
4. The MA-4P102 is available as a beam lead or a conventionally packaged chip.

FIGURE 11.4-3 STANDARD PINS

Model Number	MA-4P101	MA-4P102	MA-4P103	MA-4P202	MA-4P203	MA-4P303	MA-4P404	MA-4P504
Beam Lead	129	129	— —	— —	— —	— —	— —	— —
Chip	— —	134	134	134	134	134	134	131*
Axial Glass	— —	54	54	54	54	54	54	4
Ceramic	— —	30	30	30	30	30	30	30
Copper Heat Sink	— —	— —	— —	— —	— —	— —	— —	— —

Model Number	MA-4P505	MA-4P506	MA-4P604	MA-4P606	MA-4P607	MA-4P608	MA-4P709
Beam Lead	— —	— —	— —	— —	— —	— —	— —
Chip	131*	131*	131*	131*	212*	130*	223*
Axial Glass	4	4	4	4	— —	— —	— —
Ceramic	30	30	30	30	43/109	43/109	— —
Copper Heat Sink	— —	— —	— —	— —	150	150	150

*Available as hermetically sealed chips (CERMACHIP™)

FIGURE 11.4-4 STANDARD PIN DIODE CASE STYLE OPTIONS

11.5 MAXIMUM RATINGS

Temperature Range
Operating —65 to +175°C
Storage —65 to +200°C

CW Power Dissipation (Watts) @ $T_{op} = \frac{175 - T_{op}}{\theta_{jc}}$

where:
T_{op} = Operating Temperature (°C)
θ_{jc} = Thermal Resistance (°C/W)

11.6 RELIABILITY

Microwave Associates standard PIN diodes are capable of passing the most vigorous reliability and environmental testing in either chip or package form. For certain high volume PIN diodes, JAN and JAN TX screened versions of commercial diodes are available. For most microwave PIN diodes, there are no standard high reliability versions available. Instead, customers must write their own test and screening specifications for each individual device, and we will be glad to assist you in this procedure.

Microwave Associates is now offering all of its standard PIN diodes as commercial grade parts or with one of four levels of reliability screening. The test programs used for the diodes follow MIL-S-19500 very closely. The standard reliability designations and their meanings are as follows:

Designation	Meaning
TX	Diode has 100% preconditioning and screening per Table 11-A.
TXB	TX level testing with a sample submitted through Group B testing per Table 11-B.
TXV	TX level testing with an internal visual inspection on 100% of the parts.
TXVB	TXV level testing with a sample submitted through group B testing per Table 11-B.

To order a standard PIN diode with a standard high reliability screening, the screening level designation should be added to the end of the standard part number. For example, an MA-4P303 chip in a case style 30 ceramic package with TXV level screening would be designated as MA-4P303-30-TXV.

MIL-STD-750
TABLE 11-A TYPICAL 100% PRECONDITIONING AND SCREENING PROGRAM FOR TX LEVEL SCREENING[1]

Inspection	Method	Condition
Internal Visual and/or X-Ray	2072/ 2076	See Note 2
High Temperature Life	1032	48 hrs min at max. storage temp.
Thermal Shock	1051	10 cycles
Constant Acceleration	2006	20,000 g's, Y_1
Fine Leak	1071	H
Gross Leak	1071	C or E
Electrical	— —	See Note 3
Burn-in	1038	See Note 3
Electrical	— —	See Note 3
Stability Verification	— —	See Note 3

NOTES:
1. Test plan shown is for a packaged diode. Screening plans for chip diodes available on request.
2. Internal visual on TXV and TXVB screening programs only. X-ray is optional for any screening plan.
3. Conditions and details of tests depend on specific part number. Information available on request.

MIL-STD-750
TABLE 11-B TYPICAL SAMPLING PROGRAM FOR TXB OR TXVB PARTS[1]

Inspection	Method	Condition	LTPD
Subgroup 1			
Physical Dimensions	2066	— — —	10 — 20
Subgroup 2			
Solderability	2026		
Thermal Shock	1051	10 cycles	10 — 20
Thermal Shock	1056	A	
Hermetic Seal	1071	Condition H, C or E	
Moisture Resistance	1021		
Electrical	— —	See Note 2	
Subgroup 3			
Shock	2016	1500 g's, ½ms, 5 x @ X, Y_1 Y_2	
Vibration, Variable Freq.	2056		
Constant Acceleration	2006	20,000 g's @ X, Y1, Y2	10 — 20
Electrical	— —	See Note 2	
Subgroup 4			
Terminal Strength	2036	E	10 — 20
Subgroup 5			
High Temperature Life	1031	Max. storage temp.	$\lambda = 5$
Electrical	— —	See Note 2	
Subgroup 6			
Operating Life	1026	See Note 2	$\lambda = 5$
Electrical	— —	See Note 2	

NOTES:
1. Test plan is for a packaged diode. Programs for chips are available on request.
2. Conditions and details of tests depend on specific part number. Information available on request.

11.7 SPECIFICATIONS FOR STANDARD PINS

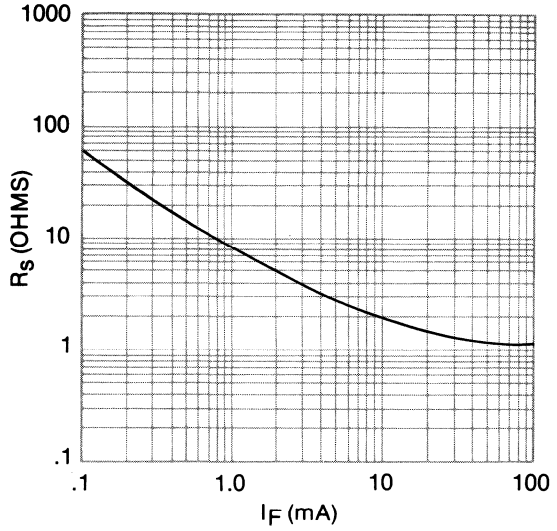
MODEL NUMBER	MA-4P101 Beam Lead	MA-4P102 -129 Beam Lead	MA-4P102	MA-4P103	MA-4P202	MA-4P203	MA-4P303	MA-4P404
CASE STYLE	129	129	30	30	30	30	30	30
Minimum V_B[1] (Volts)	40	40	50	30	100	100	200	300
Maximum C_j[2] @ V_R (pF)(Volts)	.02 @ 10	.05 @ 10	.05 @ 10	.15 @ 10	.05 @ 10	.15 @ 10	.15 @ 10	.20 @ 50
Maximum R_S[3] @ I_F (Ohms)(mA)	8 @ 10	6 @ 10	2.5 @ 10	1.5 @ 20	2.0 @ 10	1.5 @ 10	1.5 @ 10	0.6 @ 50
Typical τ_L[4] (μs)	.200	.200	.100	.010	.100	.100	.200	1.0
Typical T_{rr}[5] (μs)	.003	.003	.005	.001	.005	.020	.065	.140
Maximum θ_{jc} (°C/Watt)	600	600	60	40	60	30	30	20

MODEL NUMBER	MA-4P504	MA-4P505	MA-4P506	MA-4P604	MA-4P606	MA-4P607	MA-4P608	MA-4P709
CASE STYLE	30	30	30	30	30	43	43	150
Minimum V_B[1] (Volts)	500	500	500	1000	1000	1000	1000	1500
Maximum C_j[2] @ V_R (pF)(Volts)	.20 @ 100	.35 @ 100	.70 @ 100	.30 @ 100	.60 @ 100	1.3 @ 100	2.5 @ 100	3.3 @ 100
Maximum R_S[3] @ I_F (Ohms)(mA)	0.6 @ 100	4.5 @ 100	0.3 @ 100	1.2 @ 100	0.7 @ 100	0.4 @ 100	.35 @ 100	.35 @ 200
Typical τ_L[4] (μs)	2.0	2.0	3.0	3.0	4.0	5.0	5.0	8.0
Typical T_{rr}[5] (μs)	.350	.350	.350	.700	1.0	1.5	1.5	2
Maximum θ_{jc} (°C/Watt)	20	15	10	20	10	7	5	2

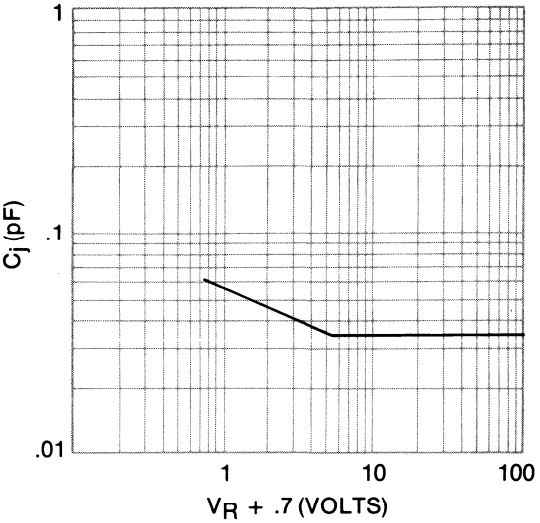
NOTES:

1. Breakdown voltage is measured at 10μA.
2. Capacitance is measured at 1 MHz.
3. Series resistance, R_S, is measured at 500 MHz.
4. Minority carrier lifetime, τ_L, is determined at the 90% recovery point with I_F = 10 mA and I_R = 6 mA.
5. Reverse recovery time, T_{rr}, is determined at the 90% recovery point with I_F = 20 mA and I_R = 200 mA.

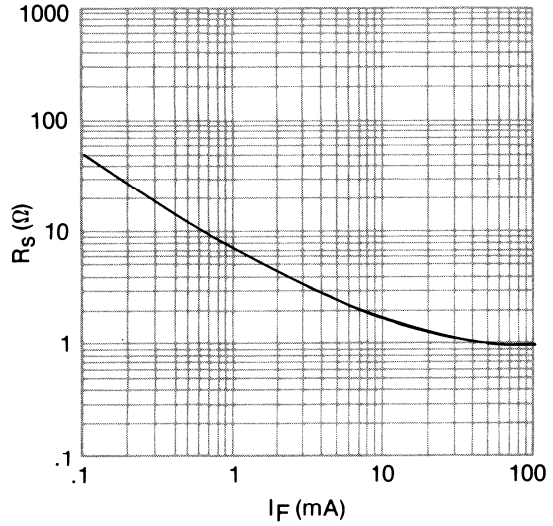
product overview



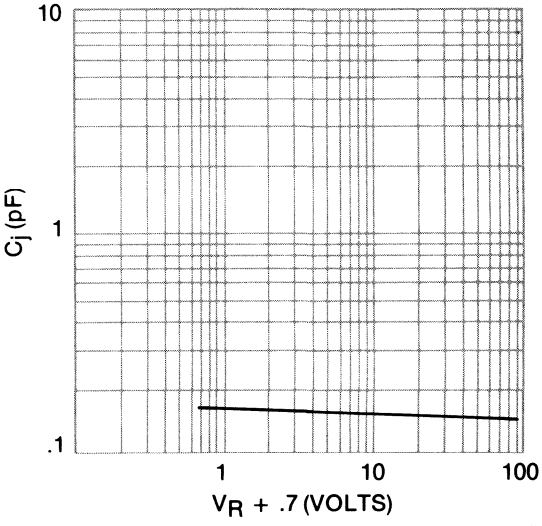
SERIES RESISTANCE, R_S, VS FORWARD CURRENT, I_F, FOR AN MA-4P102 OR MA-4P202 PIN DIODE



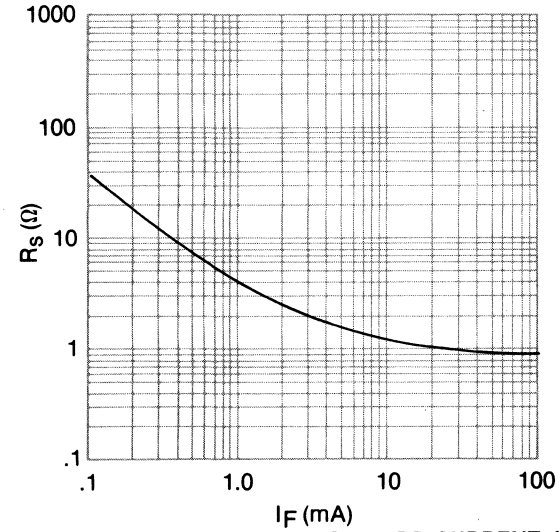
JUNCTION CAPACITANCE, C_j, VS REVERSE VOLTAGE, V_R, FOR AN MA-4P102 OR MA-4P202 PIN DIODE



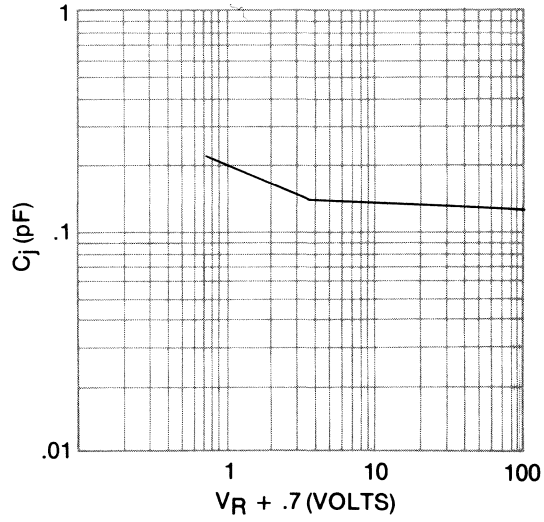
SERIES RESISTANCE, R_S, VS FORWARD CURRENT, I_F, FOR AN MA-4P103 PIN DIODE



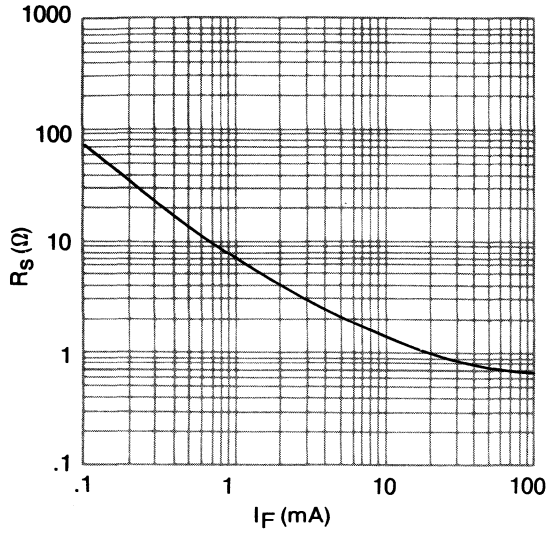
JUNCTION CAPACITANCE, C_j, VS REVERSE VOLTAGE, V_R, FOR AN MA-4P103 PIN DIODE



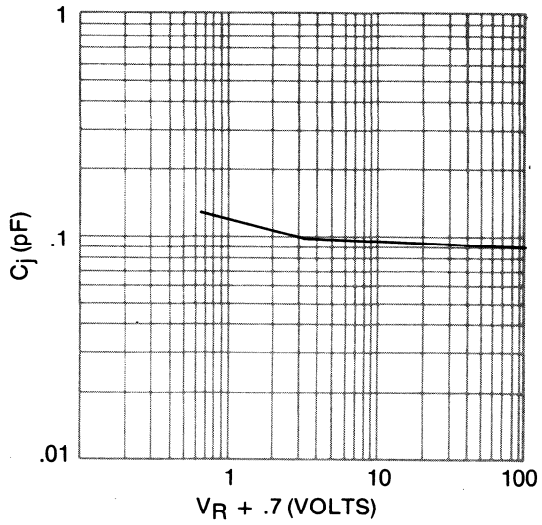
SERIES RESISTANCE, R_S, VS FORWARD CURRENT, I_F, FOR AN MA-4P203 PIN DIODE



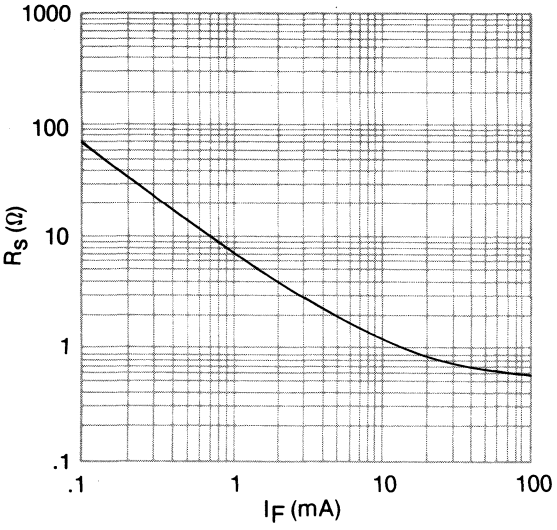
JUNCTION CAPACITANCE, C_j, VS REVERSE VOLTAGE, V_R, FOR AN MA-4P203 PIN DIODE



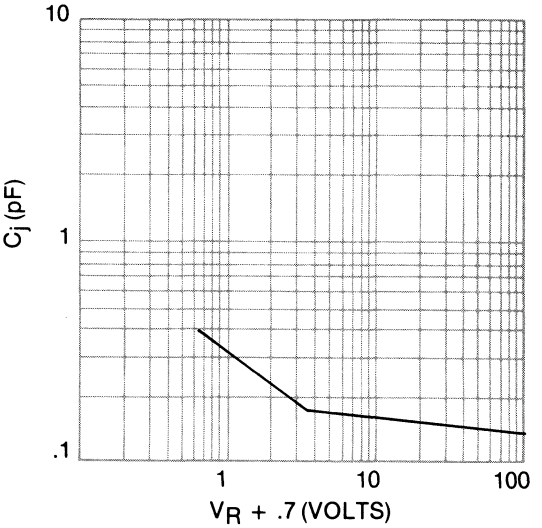
SERIES RESISTANCE, R_S, VS FORWARD CURRENT, I_F, FOR AN MA-4P303 PIN DIODE



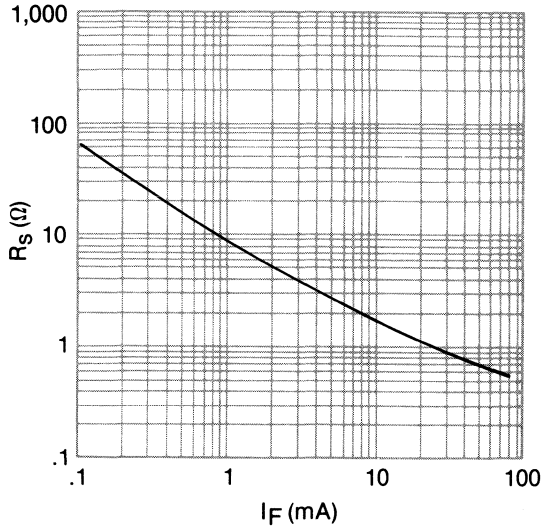
JUNCTION CAPACITANCE, C_j, VS REVERSE VOLTAGE, V_R, FOR AN MA-4P303 PIN DIODE



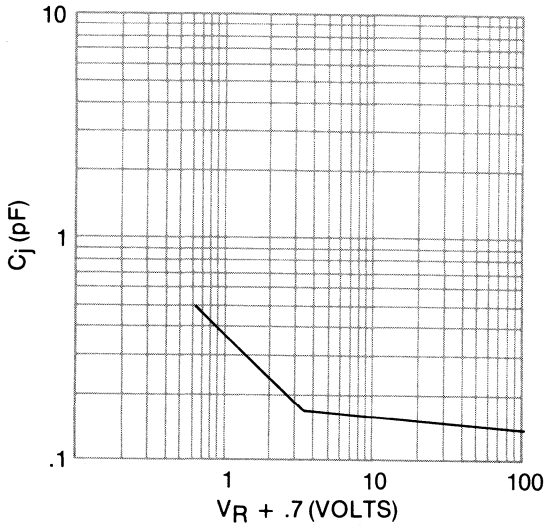
SERIES RESISTANCE, R_S, VS FORWARD CURRENT, I_F, FOR AN MA-4P404 PIN DIODE



JUNCTION CAPACITANCE, C_j, VS REVERSE VOLTAGE, V_R, FOR AN MA-4P404 PIN DIODE

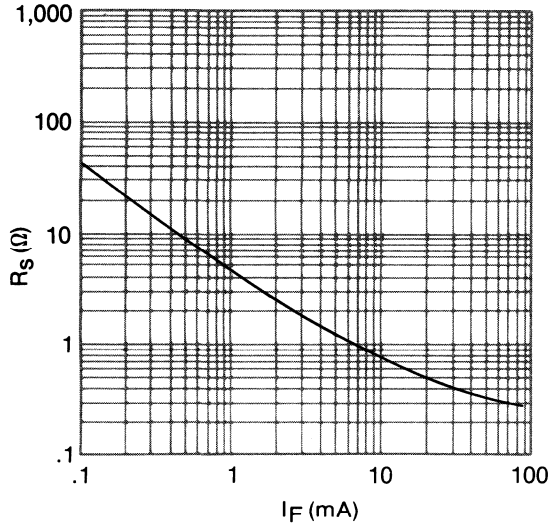


SERIES RESISTANCE, R_S, VS FORWARD CURRENT, I_F, FOR AN MA-4P504 PIN DIODE

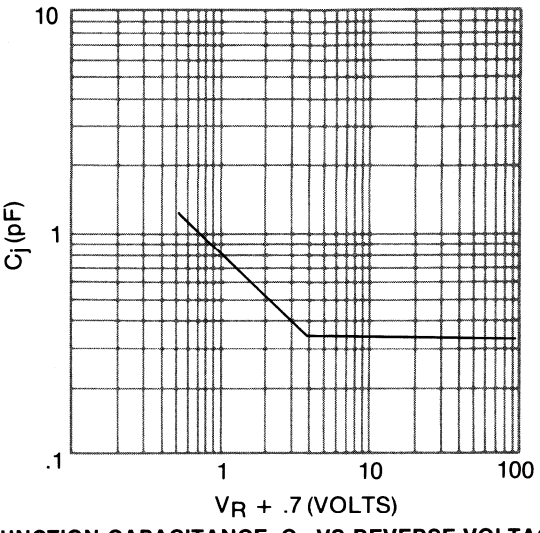


JUNCTION CAPACITANCE, C_j, VS REVERSE VOLTAGE, V_R, FOR AN MA-4P504 PIN DIODE

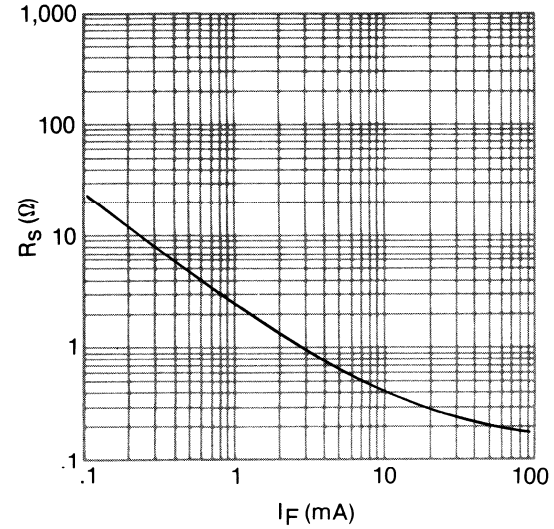
product overview



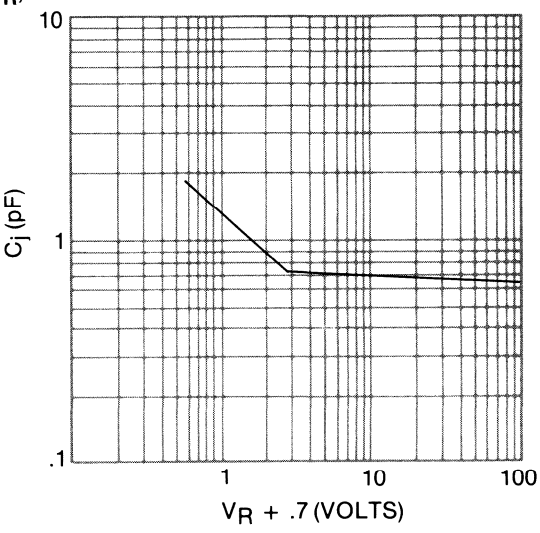
SERIES RESISTANCE, R_S, VS FORWARD CURRENT, I_F, FOR AN MA-4P505 PIN DIODE



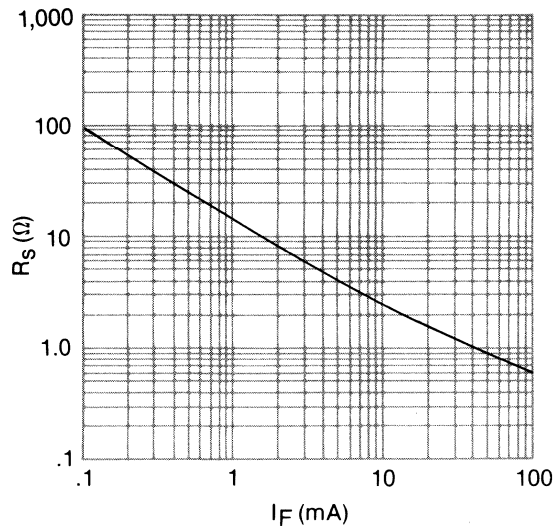
JUNCTION CAPACITANCE, C_j, VS REVERSE VOLTAGE, V_R, FOR AN MA-4P505 PIN DIODE



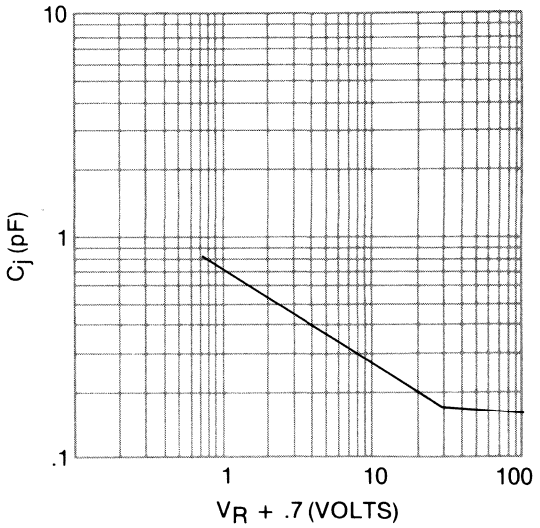
SERIES RESISTANCE, R_S, VS FORWARD CURRENT, I_F, FOR AN MA-4P506 PIN DIODE



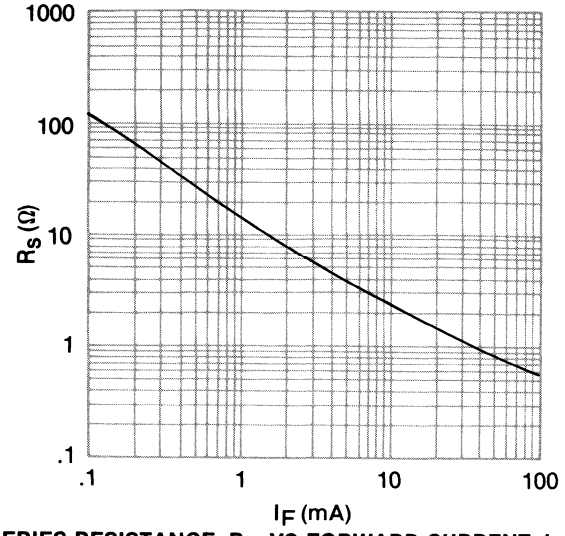
JUNCTION CAPACITANCE, C_j, VS REVERSE VOLTAGE, V_R, FOR AN MA-4P506 PIN DIODE



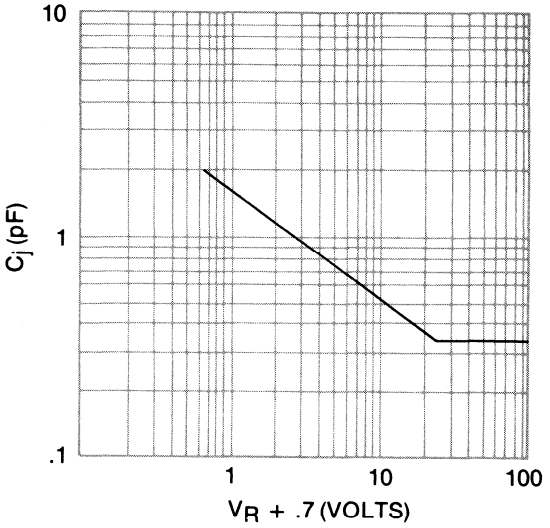
SERIES RESISTANCE, R_S, VS FORWARD CURRENT, I_F, FOR AN MA-4P604 PIN DIODE



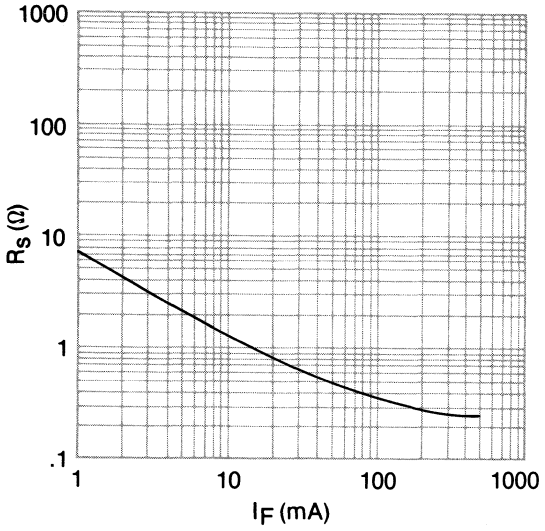
JUNCTION CAPACITANCE, C_j, VS REVERSE VOLTAGE, V_R, FOR AN MA-4P604 PIN DIODE



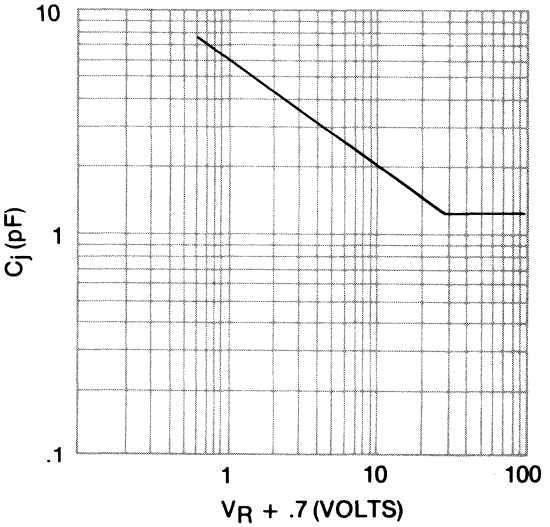
SERIES RESISTANCE, R_S, VS FORWARD CURRENT, I_F, FOR AN MA-4P606 PIN DIODE



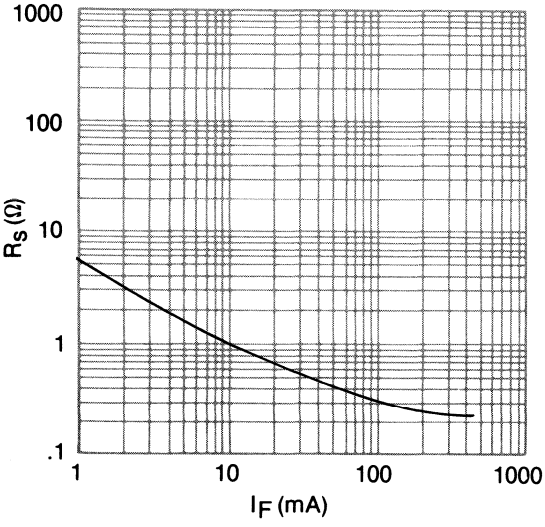
JUNCTION CAPACITANCE, C_j, VS REVERSE VOLTAGE, V_R, FOR AN MA-4P606 PIN DIODE



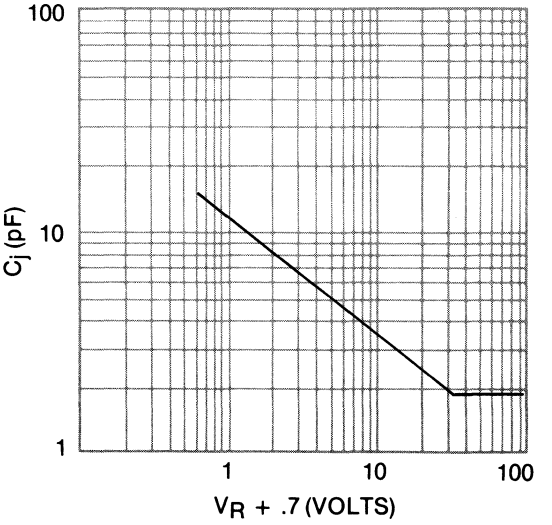
SERIES RESISTANCE, R_S, VS FORWARD CURRENT, I_F, FOR AN MA-4P607 PIN DIODE



JUNCTION CAPACITANCE, C_j, VS REVERSE VOLTAGE, V_R, FOR AN MA-4P607 PIN DIODE

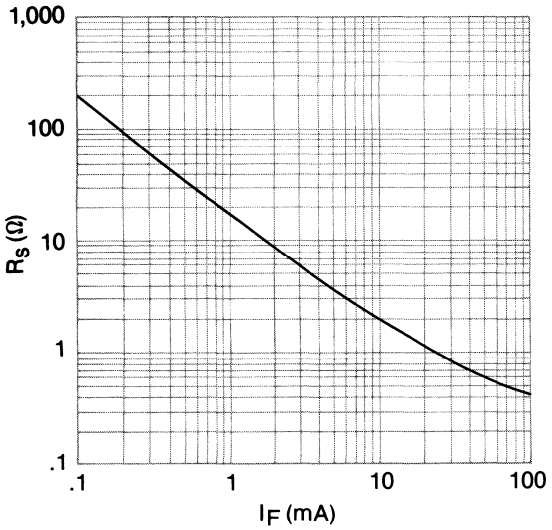


SERIES RESISTANCE, R_S, VS FORWARD CURRENT, I_F, FOR AN MA-4P608 PIN DIODE

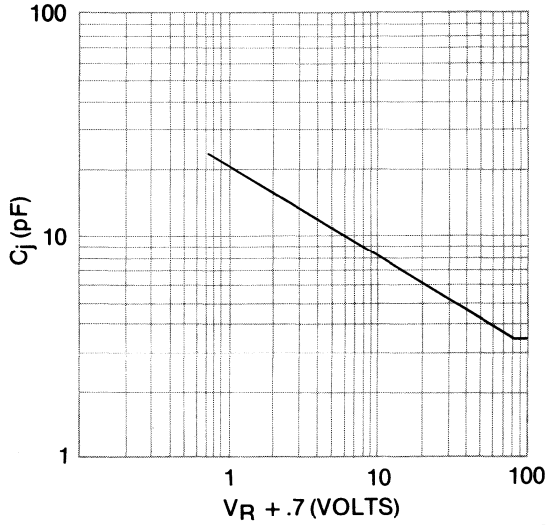


JUNCTION CAPACITANCE, C_j, VS REVERSE VOLTAGE, V_R, FOR AN MA-4P608 PIN DIODE

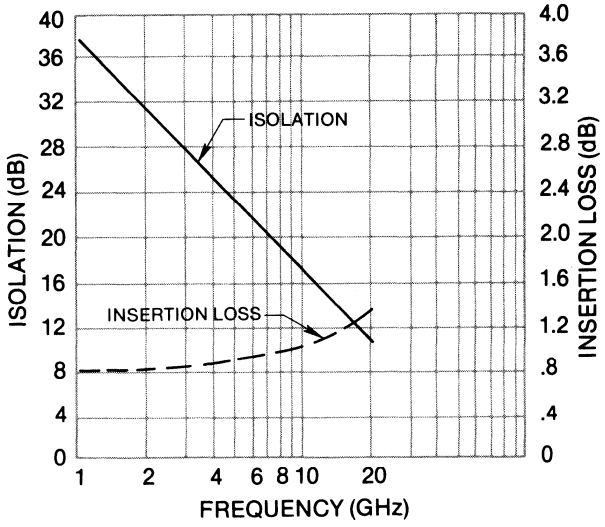
product overview



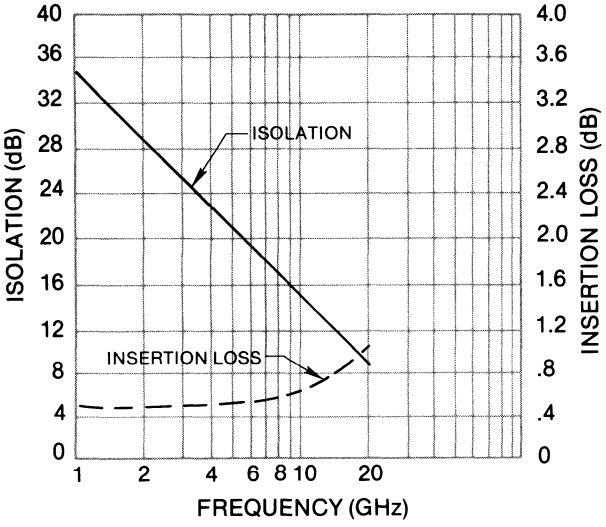
SERIES RESISTANCE, R_S, VS FORWARD CURRENT, I_F, FOR AN MA-4P709 PIN DIODE



JUNCTION CAPACITANCE, C_j, VS REVERSE VOLTAGE, V_R, FOR AN MA-4P709 PIN DIODE



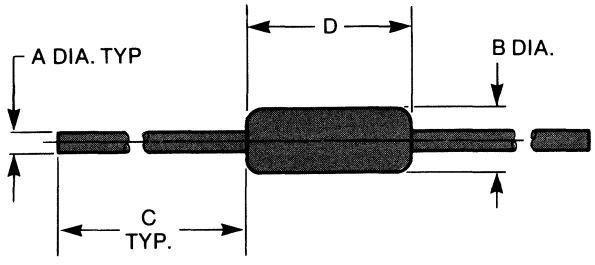
ISOLATION AND INSERTION LOSS FOR MA-4P101 USED IN A SPST SERIES SWITCH



ISOLATION AND INSERTION LOSS FOR MA-4P102 USED IN A SPST SERIES SWITCH

11.9 CASE STYLES

4



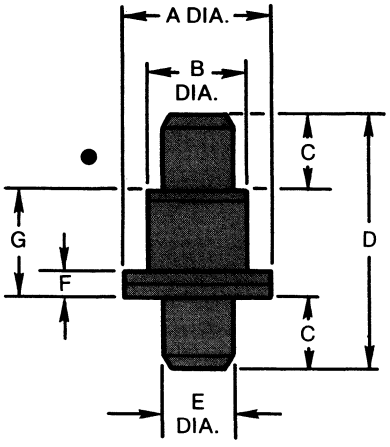
DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.018	0.022	0,46	0,56
B	0.085	0.107	2,16	2,72
C	1.000	— —	25,40	— —
D	0.230	0.300	5,84	7,62

Typ. Cp = .07 pF, Typ. L_S = 2.5 nH

Not to Scale

11.9 CASE STYLES (Cont'd)

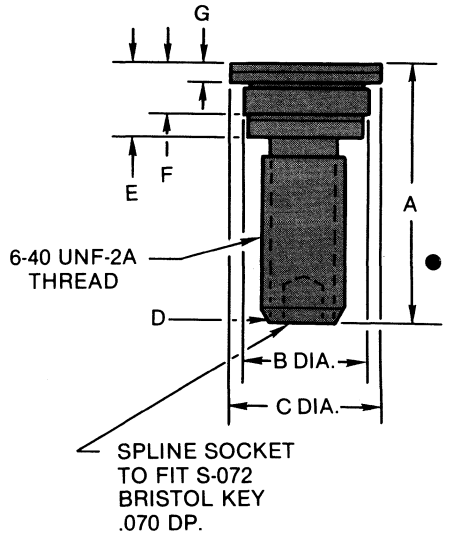
30



DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.119	0.127	3,02	3,23
B	0.079	0.083	2,01	2,11
C	0.060	0.064	1,52	1,63
D	0.205	0.225	5,21	5,72
E	0.060	0.064	1,52	1,63
F	0.016	0.024	0,41	0,61
G	0.085	0.097	2,16	2,46

Typ. Cp = .18 pF, Typ. L_S = 0.4 nH

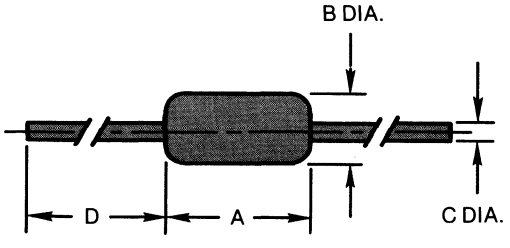
43



DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.440	0.460	11,18	11,68
B	0.208	0.212	5,28	5,38
C	0.255	0.265	6,48	6,73
D	.020 x 45° REF.		0,51 x 45° REF.	
E	0.119	0.131	3,02	3,33
F	0.050 REF.		1,27 REF.	
G	0.025	0.035	0,64	0,89

Typ. Cp = .75 pF, Typ. L_S = 0.6 nH

54



DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.145	0.165	3,68	4,19
B	0.068	0.075	1,72	1,91
C	0.014	0.016	0,35	0,41
D	1.000	1.500	25,40	38,10

Typ. Cp = .05 pF, Typ. L_S = 1.0 nH

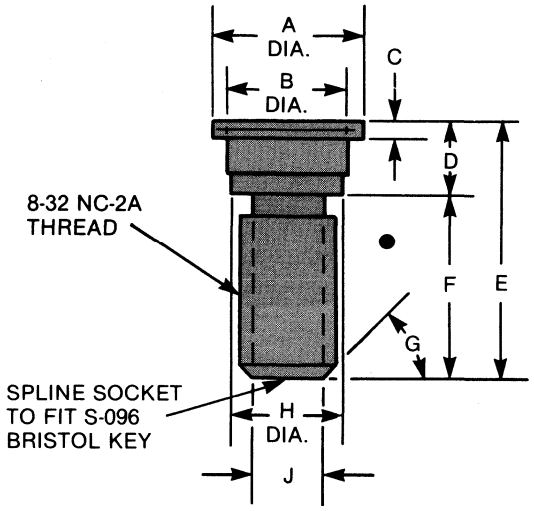
● DENOTES CATHODE END

Not to Scale

156

11.9 CASE STYLES (Cont'd)

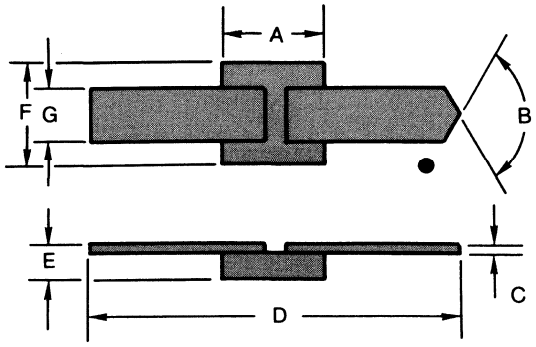
109



DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.259	0.267	6,58	6,78
B	0.207	0.213	5,26	5,41
C	0.027	0.033	0,69	0,84
D	0.118	0.134	3,00	3,40
E	0.446 REF.		11,33 REF.	
F	0.317	0.323	8,05	8,20
G	40°	50°	40°	50°
H	0.193	0.199	4,90	5,05
J	0.110	0.130	2,79	3,30

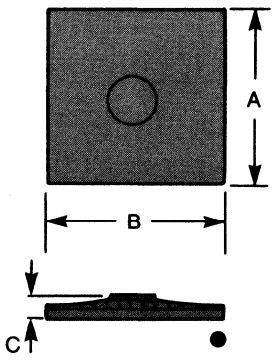
Typ. Cp = 0.75 pF, Typ. L_S = 0.75 nH

129



DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.007	0.011	0,18	0,28
B	120° NOM.		120° NOM.	
C	0.0004	0.0006	0,010	0,015
D	0.030	0.034	0,76	0,86
E	0.002	0.004	0,05	0,10
F	0.007	0.011	0,18	0,28
G	0.0045	0.0055	0,114	0,140

130



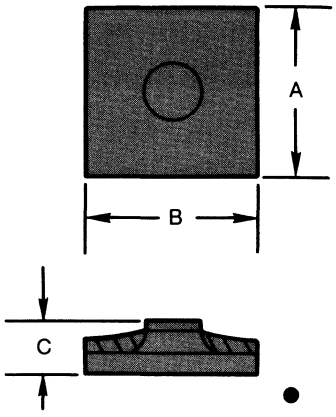
DIM.	INCHES MIN.	INCHES MAX.	MM MIN.	MM MAX.
A	0.075	0.095	1,91	2,54
B	0.075	0.095	1,91	2,54
C	0.0085	0.0105	0,216	0,267

● DENOTES CATHODE END

Not to scale

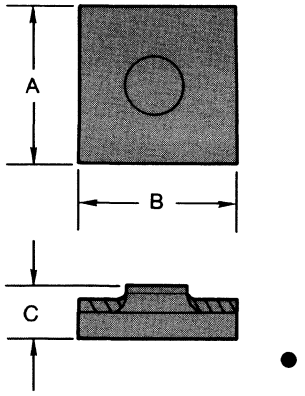
11.9 CASE STYLES (Cont'd)

131



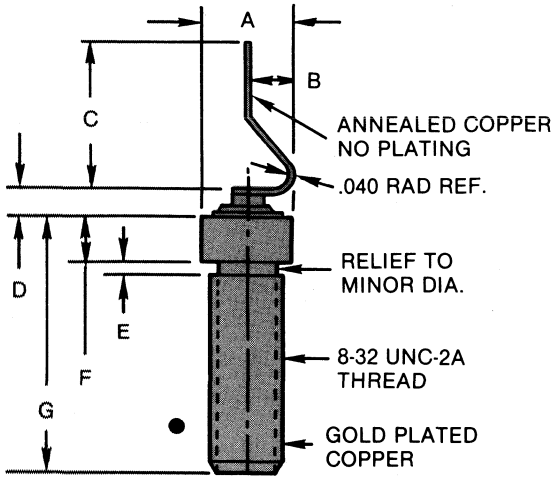
DIM.	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	0.030	0.035	0,76	0,89
B	0.030	0.035	0,76	0,89
C	0.0085	0.0105	0,216	0,267

134



DIM.	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	0.0135	0.0165	0,343	0,419
B	0.0135	0.0165	0,343	0,419
C	0.0035	0.0065	0,089	0,165

150



DIM.	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	0.180	0.190	4,57	4,83
B	0.070	0.110	1,78	2,79
C	0.300	0.360	7,62	9,14
D	0.048 REF.		1,22 REF.	
E	0.020	0.040	0,51	1,02
F	0.095	0.105	2,41	2,76
G	0.730	0.770	18,54	19,56

Typ. C_p = .04 pF, Typ. L_S = 0.8 nH

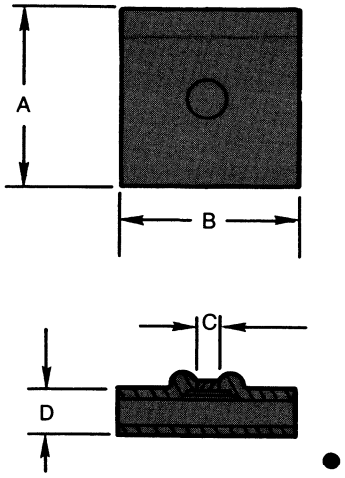
● DENOTES CATHODE END

Not to scale

158

11.9 CASE STYLES (Cont'd)

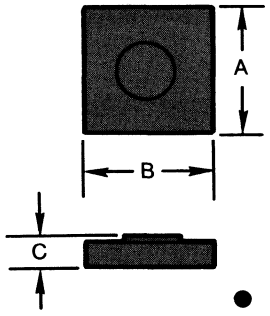
212



●

DIM.	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	0.060	0.070	1,52	1,78
B	0.060	0.070	1,52	1,78
C	0.040	0.050	1,02	1,27
D	0.010	0.015	0,25	0,38

223



●

DIM.	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	0.110	0.130	2,79	3,30
B	0.110	0.130	2,79	3,30
C	0.003	0.006	0,08	0,15

● DENOTES CATHODE END Not to Scale

notes

appendices

appendices

HOW TO ORDER — UNITED STATES — MICROWAVE ASSOCIATES.

Orders for Microwave Associates products may be placed with either our sales representatives or directly with Microwave Associates' sales department. When ordering, use Microwave Associates model number-package number. (Example: MA-42001-509.)
Microwave Associates, Inc.
Northwest Industrial Park
Burlington, Massachusetts 01803
Telephone: (617) 272-3000
TWX: 710-332-6789
TELEX: 94-9464

HOW TO ORDER — INTERNATIONAL.

Customers outside the United States are served by Microwave Associates subsidiaries: Microwave Associates International, Inc. and Microwave Associates, Ltd., as well as by international sales representatives.

MICROWAVE ASSOCIATES INTERNATIONAL.

All international orders (excluding the United Kingdom) may be placed with either our international sales representatives or directly with Microwave Associates International sales department:
Microwave Associates International, Inc.
Northwest Industrial Park
Burlington, Massachusetts 01803
Telephone: (617) 272-3000
TWX: 710-332-6789. TELEX: 094-9464
Cable: MICROWAVE BURLINGTON

UNITED KINGDOM.

Orders in the United Kingdom may be placed directly with Microwave Associates, Ltd. sales department.
Microwave Associates, Ltd.
Humphreys Road, Dunstable: Woodside Estates
Dunstable, Bedfordshire, England
Telephone: Dunstable 601441
TELEX: 82295
Cable: MICROWAVE LUTON

SHIPPING INSTRUCTIONS.

Shipments will be made via parcel post or express, whichever is less expensive, unless other instructions are received. For rush service, we will ship by Air Freight, Air Express or Air Parcel Post on request.

PRICES AND TERMS.

The price and delivery of any item in this catalog is available from either our sales department or Microwave Associates sales department. Quotations are F.O.B. factory of origin, and are subject to change without notice. Terms are net 30 days if credit has been extended. All chip sales are guaranteed 80% for RF performance and appearance. Minimum chip order is 10 pieces.

GOVERNMENT SOURCE INSPECTION.

Government source inspection is available on any item upon receipt of the complete written confirmation of purchase order items, including the prime government contract number. Government source inspection with respect to some products increases unit price and extends delivery because of duplicate standard final inspection and testing. It is recommended wherever possible that a Certificate of Compliance be substituted for government source inspection to minimize price and delivery delay.

RETURNED MATERIAL.

When returning material for repair or replacement, it is necessary first to contact the sales department. We require that complete information be included with the shipment giving a detailed description of the reason for its return, the date and purchase order on which it was obtained, the number of hours of operational use, and the exact address to which the material is to be re-shipped. All chip returns are on a lot-to-lot basis.

WARRANTY.

We warrant to the original purchaser all products sold by us to be free of defects in material and workmanship for 1 year. Our obligation under this warranty is limited to repair, exchange or credit. The warranty does not apply to any product which has been subject to accident, alteration or abuse. Detailed warranty provisions appear on each sales order.

APPLICATION ENGINEERING.

Microwave Associates maintains a large support staff of technical sales engineers, both domestically and internationally, who are expert in specific areas of microwave technology. Each has an engineering background that combines formal engineering education with training in microwave specialties — often with many years of product design experience. As further technical support, Microwave Associates makes available the services of its engineering and scientific staff who may be consulted on more advanced circuit designs or application problems.

SPECIFICATIONS.

We reserve the right to discontinue items and change specifications without notice.

FEDERAL SUPPLY CODE.

Microwave Associates' Federal Supply Code for Manufacturers assigned number is 96341.

appendices

NORTHEAST
NEW ENGLAND

Burlington Sales, Inc.
97 Cambridge Street
Burlington, MA 01803
Tel. (617) 272-7655

MIDDLE ATLANTIC
UPSTATE NEW YORK

T² Electronics Co., Inc.
4054 Newcourt Avenue
Syracuse, NY 13206
Tel. (315) 463-8592
TWX 710-541-0554

T² Electronics Co., Inc.
2 E. Main Street
Victor, NY 14564
Tel. (716) 924-9101
TWX 510-254-8542

NEW YORK CITY, LONG ISLAND, NORTHERN NEW JERSEY, WESTERN CONNECTICUT

ERA, Incorporated
One Dupont Street
Plainview, NY 11803
Tel. (516) 822-9890
TWX 510-221-1849

Microwave Associates, Inc.
1408 Blackwood Clementon Road
Blackwood, NJ 08012
Tel. (609) 228-5600

WASHINGTON, D.C. MARYLAND, VIRGINIA, AND NORTH CAROLINA

Burgin-Kreh Associates, Inc.
6100 Baltimore National Pike
Baltimore, MD 21228
Tel. (301) 788-5200
TWX 710-862-1450

Burgin-Kreh Associates, Inc.
P.O. Box 268
Kingston, TN 37663
Tel. (615) 690-6100

Burgin-Kreh Associates, Inc.
P.O. Box 19510
Raleigh, NC 27609
Tel. (919) 781-1100

Burgin-Kreh Associates, Inc.
P.O. Box 4254
Lynchburg, VA 24502
Tel. (804) 239-2626

SOUTHEAST
FLORIDA, GEORGIA, ALABAMA

Microwave Associates, Inc.
2274 State Road 580
Suite H
P.O. Box 758
Dunedin, FL 33528
Tel. (813) 796-4040
(813) 796-4858

Microwave Associates, Inc.
1010 East Atlantic Blvd.
P.O. Box 856
Pompano Beach, FL 33060
Tel. (305) 943-2690

Microwave Associates, Inc.
Suite 115
14 Perimeter Park
Atlanta, GA 30341
Tel. (404) 455-3818

SOUTHWEST
TEXAS, OKLAHOMA, ARKANSAS, LOUISIANA

Microwave Associates, Inc.
811 South Central Expressway
Richardson, TX 75080
Suite 546
Tel. (214) 234-2463
TWX 910-867-4769

ARIZONA, NEW MEXICO, COLORADO, UTAH

Microwave Associates, Inc.
7336 E. Shoeman Lane, Suite 108W
Scottsdale, AZ 85251
Tel. (602) 947-5431
TWX 910-950-1281

MIDWEST
NORTHERN ILLINOIS, SOUTHERN WISCONSIN

Dekotech, Incorporated
10001 W. Grand Avenue
P.O. Box 306
Franklin Park, IL 60131
Tel. (312) 455-5100
TWX 910-227-1761

MISSOURI, KANSAS, NEBRASKA AND SOUTHERN ILLINOIS

Midtec Associates
6912 Marion
Shawnee Mission, KS 66218
Tel. (913) 441-6565

Midtec Associates
110 S. Highway 67
Florissant, MO 63033
Tel. (314) 837-5200

IOWA, MINNESOTA

Seltec Sales Corporation
P.O. Box 128
Prior Lake
Minneapolis, MN 55372

Seltec Sales Corporation
1930 St. Andrews Drive, N.E.
P.O. Box 2172
Cedar Rapids, IA 52405
Tel. (319) 393-1114
TWX 910-525-1329

INDIANA

Delesa Sales
Executive Office Park
2118 Inwood Drive, Suite 117
Ft. Wayne, IN 46805
Tel. (219) 483-9537
TWX 810-332-1407

Delesa Sales
10026 E. 21st Street
Indianapolis, IN 46229
Tel. (317) 894-3778

OHIO, MICHIGAN, WEST VIRGINIA, AND WESTERN PENNSYLVANIA

S.A.I. Marketing Corporation
P.O. Box N
Brighton, MI 48116
Tel. (313) 227-1786
TWX 810-242-1518

S.A.I. Marketing Corp.
1050 Freeport Road
Pittsburgh, PA 15238

S.A.I. Marketing Corp.
Shaker Building
3645 Warrensville Ctr. Rd.
Suite 318, Shaker Heights
Cleveland, OH 44122

S.A.I. Marketing Corp.
137 S. Main
Centerville, OH 45459

S.A.I. Marketing Corp.
4 Main Street
P.O. Box 2368
Zanesville, OH 43701

WEST COAST
WASHINGTON, OREGON

C.K. Shanks & Associates, Inc.
4110 W. Charming Way
P.O. Box 25385
Portland, OR 97225
Tel. (503) 292-5656

C.K. Shanks & Associates, Inc.
4000 Aurora Ave. North
Suite 222
Seattle, WA 98103

NORTHERN CALIFORNIA, NEVADA

Microwave Associates, Inc.
1362 Borregas Avenue
Sunnyvale, CA 94088
P.O. Box 8010
Tel. (408) 734-2320
TWX 910-339-9248

SOUTHERN CALIFORNIA

Microwave Associates, Inc.
5855 Green Valley Circle
Suite 200
Culver City, CA 90230
Tel. (213) 645-6611
TWX 910-328-6132

appendices

CANADA
MA Electronics Canada Limited
3135 Universal Drive
Mississauga, Ontario
Canada
L4X 2E7
Tel. (416) 625-4605
TELEX 610-492-4317

MA Electronics Canada Limited
7575 Trans Canada Highway
Suite 305
St. Laurent, Quebec
H4T-1V6
TELEX 05825732

ARGENTINA
Reycom Electronica SRL
Uruguay 48570 Floor "C"
1015 Buenos Aires
Argentina
Tel 46: 1741
TELEX Public Booth 9900

AUSTRALIA
Werner Electronics
Industries Pty., Ltd.
28 Gray Street
P.O. Box 98
Kilkenny, S.A. 5009
Australia
Tel 268-2766
TELEX 8-8405
CABLE AA20365M

BELGIUM, NETHERLANDS, LUXEMBURG
Microwave Associates Int'l.
176 Rue Victor Hugo
1040 Brussels
Belgium
Tel. 735-01-95
TELEX 23281
CABLE MELABSA BRUSSELS

BRAZIL
Cosele Ltda.
Rua Da Consolacao
867-Cj. 31
01301 Sao Paulo
Brazil
Tel. 259-3719
TELEX 011-30869
CABLE "SEMICHIP"

DENMARK
Tage Olsen A/S
Ballerup Byuej 222
P.O. Box 225
2750 Ballerup
Denmark
Tel. 2-658111
TELEX 35293

FINLAND
Carlo Casagrande Oy
Kalevankatu 4
Helsinki 10
Finland
Tel. 640-711
TELEX 12-1677
CABLE CARCAS HELSINKI

FRANCE
Microwave Associates, S.A.
57-59 Rue De La Convention
Paris 75015
France
Tel. 579-2338
TELEX 202100F

INDIA
Radelcom
9/3 Museum Road
Bangalore 560-001
India
Tel. 53581
TELEX 8458123

ISRAEL
Microkim Limited
Science Based Industries
Technion City, Haifa
Israel
Tel. (04) 227-181
TELEX 922-46582

ITALY
Microwave Associates Italia Srl
Via Bressanone, 5
00198 Rome
Italy (Northern)
Tel. 83 15 046, 83 65 35
TELEX 610105

Via Andrea Doria, 17
20124 Milan, Italy (Southern)
Tel. 270922
TELEX 843333258

JAPAN
Hakuto Co., Ltd.
Foreign Division
P.O. Box 25
Tokyo Central 100-91
Japan
Tel. (503) 3711-9
TELEX J22912
CABLE BRAPAN TOKYO

MEXICO
Mexitek S.A.
Eugenia 408, Dept. 1Y5
APDO Postal 12-1012
Mexico, 12, D.F.
Tel. 536-09-10 or 532-97-51

NEW ZEALAND
Amalgamated Wireless
(Australasia) N.Z., Ltd.
P.O. Box 830
Wellington, 2
New Zealand
Tel. 51-279
TELEX NZ31001

NORWAY
Norbritco A/S
P.O. Box 2582 Solli
Oslo 2
Norway
Tel. 41-59-35
TELEX 16743
CABLE BRITCO OSLO

SOUTH AFRICA
Fairmont Electronics (Pty.) Ltd.
P.O. Box 41102
Craighall 2024
Transvaal
South Africa
Tel. 789-1230/4
TELEX 4-24842 SA
CABLE "FAIRTRONICS" CRAIGHALL

SPAIN
Hispano Electronica S.A.
Poligono Industrial Urtinsa
Aptdo. de Correos 48
Alcorcon (Madrid) Spain

SWEDEN
Swedish Elektronik A/B
Box 566
191 05 Sollentuna
Sweden
Tel. 08-96-7660
TELEX 13461 S. Swelink
CABLE TELELINK STOCKHOLM

SWITZERLAND
Technology Resources AG
Bubenbergplatz 10
CH-3011
Bern
Switzerland
Tel. (031) 22-39-73
TELEX 33450

TAIWAN, HONG KONG
Shigma, Inc. (Taiwan Branch)
Room 404, 4th Floor, Q Bldg.
152 Chung Shan N Road, Sec. 1
Taipei
Taiwan
Tel. 5614300, 4309, 0148 & 0149
TELEX 22590 Shigma

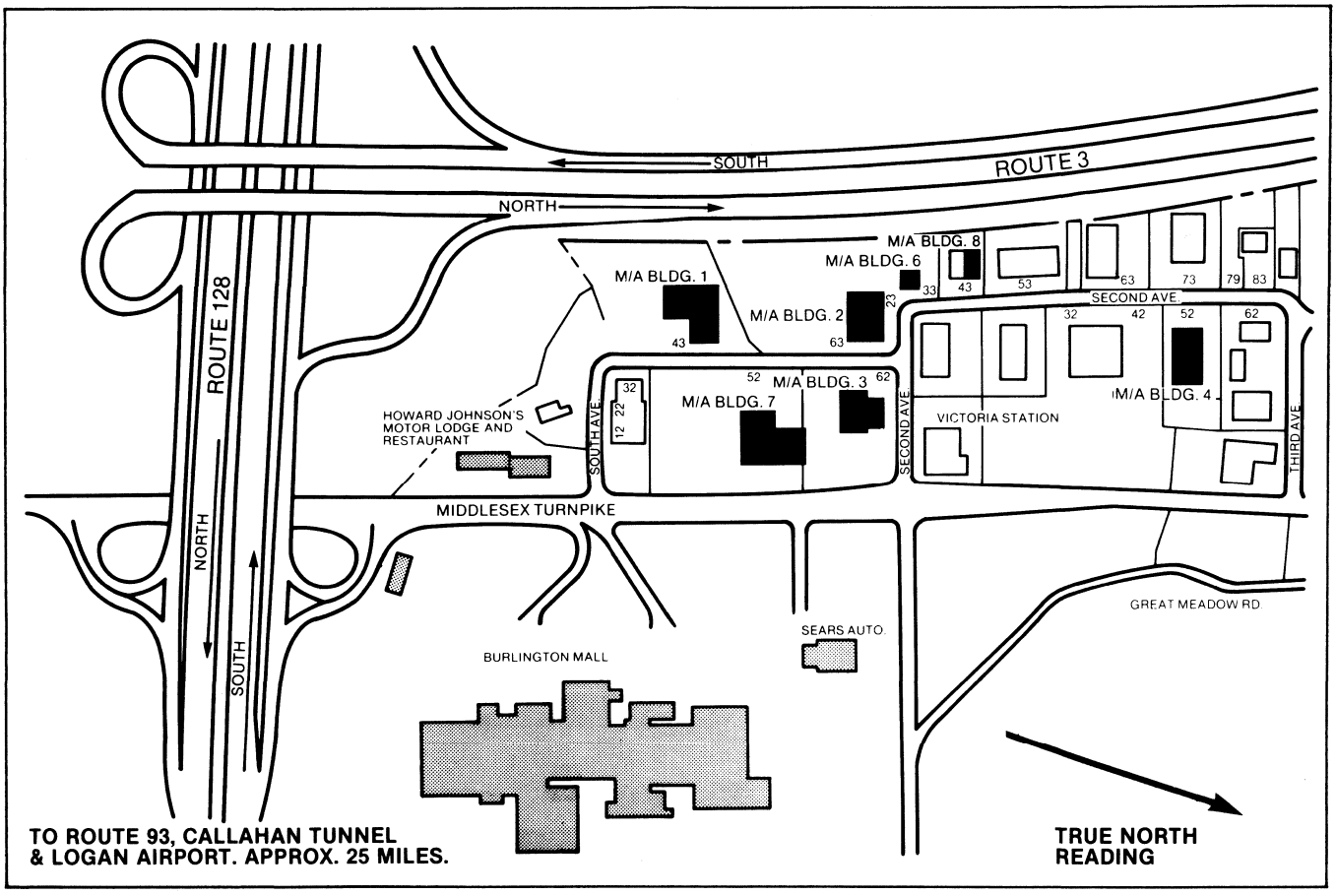
UNITED KINGDOM
Microwave Associates, Ltd.
Dunstable LU5 4SX
Bedfordshire
England
Tel. 582-601441
TELEX 82295
CABLE MICROWAVE DUNSTABLE

WEST GERMANY & AUSTRIA
Microwave Associates, GmbH
Weltenburger Strasse 33
D-8 Munchen 80
West Germany
Tel. 089-91-2360
TELEX 5-29103 MAGM

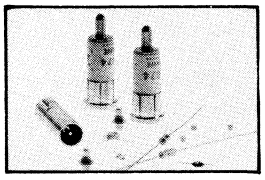
EASTERN EUROPE, EAST GERMANY, POLAND, HUNGARY, BULGARIA, RUMANIA, YUGOSLAVIA, CZECHOSLOVAKIA, U.S.S.R.
Microwave Associates Int'l.
19a Creffield Road, Ealing,
London, W5 3RR
England
Tel. 992-6396
TELEX 82295
CABLE MUWAVE LONDON W5
London W5
England

appendices

164

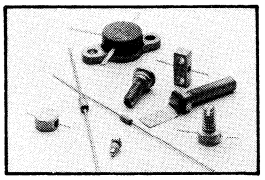


MICROWAVE SEMICONDUCTORS



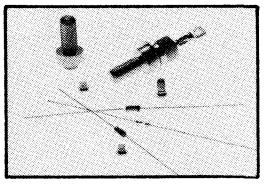
SCHOTTKY & POINT CONTACT DIODES

- Low-noise Schottky Barrier Diodes for mixer/detector/modulator applications
- Gallium Arsenide Diodes for millimeter applications
- Schottky Barrier Beam Leads and Quads
- Broadband Point Contact Diodes



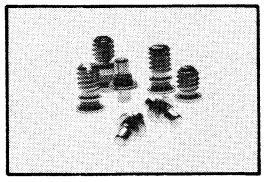
PIN DIODES

- Complete family for switching, limiter, and attenuator applications
- V_B to 2000 V available in chip, ceramic, or glass packages
- High volume glass package products for VHF/UHF applications
- "Cermachip" hermetically sealed PIN chips



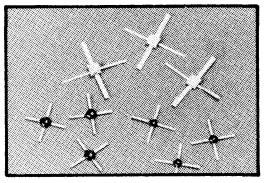
VARACTOR DIODES

- Both GaAs and Silicon in most package styles
- Broad line of Multiplier Varactors
- Abrupt and Hyperabrupt Junction Tuning Varactors



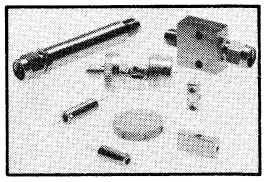
IMPATTS & GUNN DIODES

- Impatts with P_O >25W with 1 μs pulse
- Impatts with P_O = 5W CW
- GaAs Gunn Diodes for motion detection, military and commercial sources, and telecommunications to 1W P_O



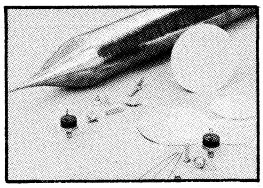
TRANSISTORS

- Low-noise, broadband, high reliability transistors for general purpose and wide-dynamic-range RF amplifiers as well as medium power oscillators.
- f_t to 8 GHz
- N.F. as low as 1 dB



MODULES & DETECTORS

- VHF to 18 GHz
- SPST through SP6T Switches
- Complete line of detectors, limiter-detectors, limiters, and attenuators



SILICON & GALLIUM ARSENIDE MATERIALS

- Silicon epitaxial wafers and substrates for discrete devices, MOS, and IC applications
- Slip-free, dislocation-free epitaxy
- Epitaxial layers from 1 micron thick and up
- 0.001 to >200 ohm-cm resistivity

Write or call for specific information about any product. Microwave Associates, Inc., Bldg. 4, South Ave., Burlington, MA 01803 (617) 272-3000

Microwave Associates
A M/A-COM COMPANY

MICROWAVE ASSOCIATES
A M/A-COM COMPANY

SOUTH AVENUE
BURLINGTON, MA 01803

(617) 272-3000